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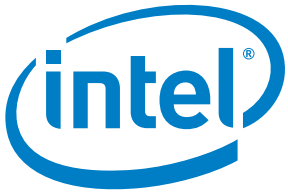

CPE Product Family

Gateway SoCs
Voice System Package 4.44 RC5

Release Note

Revision 2.0, 2017-05-31
Intel Confidential
Reference ID 617837

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Revision History

Current:	**Revision 2.0, 2017-05-31**
Previous:	**None**
Page	**Major changes since previous revision**
All	Following products have been re-branded and their names have been changed: • "XWAY™ ARX300 Family" renamed "ARX300 Family" • XWAY™ ARX388 renamed ARX388 • "XWAY™ xRX200 Family" renamed "xRX200 Family" • XWAY™ GRX288 renamed GRX288 • XWAY™ VRX288 renamed VRX288 • "XWAY™ GRX300 Family" renamed "Intel® AnyWAN™ SoC GRX300 Series" • XWAY™ GRX388 renamed PXB 4310 • "SLIC 200 Family" renamed "Intel® SLIC for CPE" • SLIC 210 renamed SLC210 • SLIC 220 renamed SLC220 • "XWAY™ SLIC100 Family" renamed "Intel® SLIC for CPE" • XWAY™ SLIC110 renamed SLC110 • XWAY™ SLIC120 renamed SLC120 • XWAY™ SLIC121 renamed SLC121 • "DUSLIC™ XS Family" renamed "Intel® Telephony Chipset for CPE, DXS Series" • DUSLIC™ XS1 renamed DXS101 • DUSLIC™ XS2 renamed DXS102
4, **5**	SLC110 (previous name XWAY™ SLIC110) Version 1.1 removed from **Preface** and **Table 2**
16	Open issue added in **Table 8** for DXS102

Preface

This document describes the supported features, latest changes and open issues for the Voice System Package 4.44 RC5, where “4.44 RC5” is a label for the feature set described in **Chapter 2**.

This system package is valid for the devices listed below:

- Intel® AnyWAN™ SoC GRX350 Series:
  - PXB 4395, Version 1.2
  - PXB 4395-1600, Version 1.2
- Intel® AnyWAN™ SoC GRX550 Series:
  - PXB 4583-2000, Version 1.2
- ARX300 Family:
  - ARX388 (PSB 50388), Version 1.2
- xRX200 Family:
  - GRX220 (PXB 4202), Version 1.1
  - GRX288 (PXB 4210), Version 1.2
  - VRX288 (PSB 80920), Version 1.2
- Intel® AnyWAN™ SoC GRX300 Series:
  - PXB 4310, Version 1.2
  - PXB 4387, Version 2.1
  - PXB 4389, Version 2.1
  - PXB 4389 720 MHz, Version 2.1
- VRX220 Family:
  - PSB 80221, Version 1.1
- ARX220 Family:
  - PSB 50221, Version 1.1
- Intel® SLIC for CPE:
  - SLC210 (PEF41078VV11)
  - SLC220 (PEF42078VTV11)
- Intel® SLIC for CPE:
  - SLC110 (PEF41068VV12)
  - SLC120 (PEF42068FV12, PEF42068VV12)
  - SLC121 (PEF42168VV12)
- Intel® Telephony Chipset for CPE, DXS Series:
  - DXS101 (PEF32001VV11)
  - DXS101 (PEF32001VTV12, PEF32001VV12, PEF32001VSV12)
  - DXS102 (PEF32002VTV11)
  - DXS102 (PEF32002VTV12)

1 Overview

Table 1 gives a general overview of the Gateway SoCs Voice System Package 4.44 RC5.

Table 1 General Overview of the Voice System Package 4.44 RC5

New System Package	
System Package Version	Gateway SoCs Voice System Package 4.44 RC5
System Package Software Filename	setup_Voice CPE System Package_4.44 RC5.zip
Release Date	2016-12-02
Previous System Package	
System Package Version	Gateway SoCs Voice System Package 4.44 RC4
System Package Software Filename	setup_Voice CPE System Package_4.44.zip
Release Date	2016-06-30

Table 2 gives an overview of the components of the Gateway SoCs Voice System Package 4.44 RC5. These components are available via your local technical support or sales team.

Table 2 Detailed Components of the Voice System Package 4.44 RC5

Component Type	Version	Comment
Intel® AnyWAN™ SoC GRX350 Series: PXB 4395 PXB 4395-1600	 Version 1.2 Version 1.2	For VoIP and POTS System refer to [2] or [3]
Intel® AnyWAN™ SoC GRX550 Series: PXB 4583-2000	 Version 1.2	For VoIP and POTS System refer to [2] or [3]
ARX300 Family: ARX388 (PSB 50388)	 Version 1.2	For VoIP and POTS System refer to [1], [2] or [3]
xRX200 Family GRX220 (PXB 4202) GRX288 (PXB 4210) VRX288 (PSB 80920)	 Version 1.1 Version 1.2 Version 1.2	For VoIP and POTS System refer to [1], [2] or [3]
Intel® AnyWAN™ SoC GRX300 Series: PXB 4310 PXB 4387 PXB 4389 PXB 4389 720 MHz	 Version 1.2 Version 2.1 Version 2.1 Version 2.1	For VoIP and POTS System refer to [1], [2] or [3]
VRX220 Family: PSB 80221	 Version 1.1	For VoIP and POTS System refer to [1], [2] or [3]
ARX220 Family: PSB 50221	 Version 1.1	For VoIP and POTS System refer to [1], [2] or [3]
Intel® SLIC for CPE: SLC210 (PEF41078VV11) SLC220 (PEF42078VTV11)	 Version 1.1 Version 1.1	For VoIP and POTS System refer to [2]
Intel® SLIC for CPE: SLC110 (PEF41068VV12) SLC120 (PEF42068FV12, PEF42068VV12) SLC121 (PEF42168VV12)	 Version 1.2 Version 1.2 Version 1.2	For VoIP and POTS System refer to [1] or [3]

Table 2 Detailed Components of the Voice System Package 4.44 RC5 (cont'd)

Component Type	Version	Comment
Intel® Telephony Chipset for CPE, DXS Series: DXS101 (PEF32001VV11) DXS101 (PEF32001VTV12, PEF32001VV12, PEF32001VSV12) DXS102 (PEF32002VTV11) DXS102 (PEF32002VTV12)	 Version 1.1 Version 1.2 Version 1.1 Version 1.2	For DXS System refer to [4]
TAPI High Level Driver: drv_tapi TAPI Low Level Driver: drv_vmmc, drv_vmmc_xrx500, drv_dxs TAPI VCODEC Mailbox Driver: drv_sdd_mbx TAPI QoS Driver: drv_kpi2udp	4.16.3.0 1.21.2.0 1.20.4.0 1.1.4.0 1.2.2.0 3.0.5.1	– Contains MPS 4.0.4.0 Contains MPS 3.2.4.0, SDD 2.1.2.0, Loader 1.2.0.0
GRX350/GRX550 Firmware DXS Firmware xRX300 VoIP Firmware xRX200 VoIP Firmware	1.2.6.10.0 2.0.0 2.1.0.8.0 3.5.0.7.0	Contains GRX350 VoIP Firmware 1.2.0.10.2 (voip_R1.2.0.10.2.bin) , DFEV Voice Codec Firmware 1.5.0.3 (vcodec_cimg_1_5_0_3.bin) , Voice Codec Firmware 1.6.0.5 (vcodec_cimg_1_6_0_5.bin) Contains DXS Version 1.1 Firmware 1.4.5 (dxs_fw-1.4.5.bin) , DXS101 Version 1.2 Firmware 130.1.0.3 (duslicxs1_130_1_0_3.bin), DXS102 Version 1.2 Firmware 130.1.0.3 (duslicxs2_130_1_0_3.bin)
TAPI Line Testing library: lib_lt	0.6.0.2	–
TAPI country library: lib_country	1.0.4.0	–
TAPIDEMO TAPI CLI tooling event_logger tapidump	5.9.3.0 2.3.0.1 1.8.5.0 1.1.11 1.1.1.0	For demonstration, integration support and debugging purposes - not for productive use
XTCOS	V4.4.0.0[1)]	Coefficient calculation program [7]
Example BBD files for EASY 350 VDSL oPOTS EASY 550 VDSL oPOTS EASY 550-2000 VDSL oPOTS (EASY550 2000V2)	3.0.0	–
Example BBD files for EASY 32001-IBB12 EASY 32002-IBB12 EASY 32002-CIBB12 EASY 32001-IFB12 EASY 32002-IFB12 EASY 32002-CIFB12	0.0.9	–

Table 2 Detailed Components of the Voice System Package 4.44 RC5 (cont'd)

Component Type	Version	Comment
Example BBD files for EASY 80920 and EASY 220 Boards	0.9.5	–
Example BBD files for EASY 388, EASY 300/330 VDSL BOND and EASY 300 US VDSL BOND	0.2.0	–
Voice System Package documentation	–	Refer to **Literature References**

1) Minimum requirement is XTCOS V4.4.0.0 or higher

Note: The XTCOS software is not delivered with the Voice System Package. The latest versions can be downloaded free of charge from the company website. Please contact your sales representative or local sales office if you require assistance in obtaining the required software.

Table 3 gives an overview of the UGW versions on which the Gateway SoCs Voice System Package 4.44 RC5 integration was tested and the platforms which were used together with Intel evaluation board "GRX500 EVM".

Table 3 UGW Version and Model Used for System Integration on Tested Platforms

UGW Version	UGW Model	Tested Platforms
UGW 6.1.1 for GRX350	GRX350_GW_HE_VDSL_LTE	GRX500 EVM with EASY 42078
UGW 7.2	GRX350_1600_MR_VDSL_LTE_SEC_GW_72	GRX500 EVM with EASY 42078

2 Supported Features

Table 4, Table 5 and Table 6 list the available features of the Voice System Package 4.44 RC5. SLIC features supported are only from Table 5 or Table 6, but not both at the same time.

Abbreviations used in the table: S = supported; C/R = channels/resources; Y = yes; N = no

Note: Not all hardware and firmware features may be supported by the device drivers. If there are any questions, please contact your local sales team.

Table 4 General Voice Processing Features

Feature	xRX200/ xRX300[1]		GRX350[2]/ GRX550[3]		Restrictions/Comments
	S	C/R	S	C/R	
Voice over IP					
RTP protocol support	Y	5	Y	5	–
SRTP support	N	–	Y	5	
RTCP support	Y	5	Y	5	–
Partial support of RTCP-XR (RFC3611)	Y	5	Y	5	The blocks "Statistics Summary Report" and "VoIP Metrics Report" are partially supported. See Chapter 5
G.711 incl. Appendix I (PLC) and Appendix II (VAD/CNG); 10, 20, 30, 40, 60 ms	Y	5	Y	5	PLC is sometimes called BFI
G.726 (16, 24, 32, 40 kbit/s) incl. Appendix I (PLC) and Appendix II (VAD/CNG); 10, 20, 30, 40, 60 ms	Y	5	Y	5	PLC is sometimes called BFI
G.722 (64 kbit/s); 10, 20, 30, 40, 60 ms including BFI	Y	5	Y	5	–
G.722.1 (24 kbit/s and 32 kbit/s); 10, 20, 30, 40, 60 ms	N	–	Y	5	–
G.723.1 (5.3 kbit/s and 6.3 kbit/s); 30, 60 ms	N	–	N	–	–
G.729 Annex A (8 kbit/s) and Annex B; 10, 20, 30, 40, 60 ms	Y	5	Y	5	–
iLBC (13.3 kbit/s); 30, 60 ms iLBC (15.2 kbit/s); 20, 40, 60 ms	N	–	N	–	–
AMR-NB (narrowband); 20, 40, 60 ms	N	–	Y	5	–
G.722.2 AMR-WB (wideband); 20, 40, 60 ms	N	–	N	–	–
Line Echo Cancellation exceeding G.165, G.168, G.168-2004: NLEC up to 16 ms tail length	Y	4	Y	4	–
Window based line echo cancellation up to 128 ms tail length with 8+8 ms windows (narrowband)	Y	4	Y	4	Same resources as for NLEC
Near-end line echo cancellation 4 ms (wideband)	Y	4	Y	4	–
Echo suppressor	Y	4	Y	6	Includes echo suppressor for DECT channel
Adaptive and fixed jitter buffer	Y	5	Y	5	Includes adaptation during silence (switchable via TAPI)
Automatic Gain Control (AGC)	Y	5	Y	5	–
Decoder Change Event	Y	–	Y	–	–

Table 4 General Voice Processing Features (cont'd)

Feature	xRX200/ xRX300[1]		GRX350[2]/ GRX550[3]		Restrictions/Comments
	S	C/R	S	C/R	
Announcement playout	Y	–	N	–	–
MOS-LQE estimation	Y	–	Y	–	–
Hold remote VoIP party	Y	–	Y	–	–
Clear Channel Data mode	N	–	N	–	Linear RTP packaging (8 bit)
PCM Interface					
PCM Interface G.711 A-law	Y	8	Y	8	–
PCM Interface G.711 µ-law	Y	8	Y	8	–
PCM Interface 16 bit linear	Y	8	Y	8	Narrowband only
PCM Interface G.726 support	Y	8	Y	8	–
PCM Interface G.722 wideband support	Y	8	Y	8	–
PCM Channel HDLC Mode	Y	2	N	–	Including selectable idle pattern
Connection Control Service					
3-party conferencing via packet network	Y	–	Y	–	–
3-party conferencing via PCM	Y	–	Y	–	–
3-party conferencing via PCM and packet network	Y	–	Y	–	–
Fax Relay					
T.38 version 0 (transport protocol: UDP, modulations: V.21, V.27ter, V.29 and V.17)	Y	2	Y	2	–
Signaling					
Integrated DTMF generator	Y	5	Y	5	–
Integrated DTMF receiver	Y	5	Y	5	–
Modem/Fax Tone Discriminator (MFTD)	Y	5	Y	5	–
Integrated FSK (Caller ID) generator, according to Bell 202 and V.23	Y	5	Y	5	–
Integrated FSK (Caller ID) receiver	Y	5	Y	5	–
Call Progress Tone Detection (CPTD)	Y	5	Y	5	–
RFC 4733 DTMF relay	Y	5	Y	5	Different payload types are possible for upstream and downstream; RFC 4733 obsoletes RFC 2833.
TAPI events upon RFC 4733 event packet reception	Y	5	Y	5	–
Universal Tone Generation in up/downstream (different tones)	Y	10	Y	10	Two generators per signaling module
Driver/API					
Linux* 3.10	Y	–	Y	–	–
Big endian support	Y	–	Y	–	–
Little endian support	N	–	N	–	–

Table 4 General Voice Processing Features (cont'd)

Feature	xRX200/ xRX300[1]		GRX350[2]/ GRX550[3]		Restrictions/Comments
	S	C/R	S	C/R	
Support for KPI tasklet mode	Y	–	Y	–	–
Polling access	N	–	N	–	–
Support for MIPS CPU clock scaling (for CoC)	Y	–	Y	–	–
Interface to use IOCTLs from kernel space	Y	–	Y	–	–
Support for Caller ID type 1 (on hook) sequences according to Telcordia/Bellcore, ETSI, SIN 227 (British Telecom), NTT (Japan)	Y	–	Y	–	–
Support for Caller ID type 2 (off hook) sequences according to Telcordia/Bellcore, ETSI, SIN 227 (British Telecom)	Y	–	Y	–	–
Support for Caller ID type 2 (off hook) sequences according to NTT (Japan)	Y	–	Y	–	–
Support for Caller ID sequences according to KPN	Y	–	Y	–	–
Support for Message Waiting Indication (VMWI using FSK)	Y	–	Y	–	By integrated Caller ID (FSK) generator
SLIC Types					
Intel® SLIC for CPE: SLC110, SLC120, SLC121	Y	–	Y	–	–
Intel® SLIC for CPE: SLC210, SLC220	N	–	Y	–	–
Intel® Telephony Chipset for CPE, DXS Series: DXS101, DXS102	N	–	Y	–	–

1) Devices of the ARX300, xRX200, GRX300, VRX220 and ARX220 Families
2) PXB 4395 Version 1.2, PXB 4395-1600 Version 1.2, devices of the GRX350 Series
3) PXB 4583-2000 Version 1.2, device of the GRX550 Series

Table 5 Intel® SLIC for CPE Supported Features

Feature	xRX200/ xRX300[1]		GRX350[2]/ GRX550[3]		Restrictions/Comments
	S	C/R	S	C/R	
CODEC/SLIC					
Worldwide programmability for AC transmission performance parameters (country specific programming, e.g. AC impedance matching, hybrid balance, transmit and receive gain, frequency response), specification in accordance with ITU-T Recommendation Q.552 for interface Z and ETSI Standard ES 202 971	Y	–	Y	–	–
Integrated sinusoidal balanced ringing capability, software programmable up to 65 Vrms ringing voltage (depending on external components), frequency range between 15 and 60 Hz	Y	2	Y	2	–
Loop start signaling	Y	2	Y	2	–
Polarity reversal	Y	2	Y	2	–
Programmable 12/16 kHz metering pulse generation (teletax, TTX) and integrated notch filtering	Y	2	Y	2	–
AC Ring Trip detection	Y	2	Y	2	–
DC Ring Trip detection	Y	2	Y	2	–
Fast Ring Trip detection	Y	2	Y	2	–
Ringing with DC offset	Y	2	Y	2	–
On-hook transmission	Y	2	Y	2	–
Wideband support (16 kHz transmission possible)	Y	–	Y	–	–
Integrated Test and Diagnostic Functions for local loop monitoring according to GR-909	Y	–	Y	–	All five measurements must be selected in Ifxphone_LT_GR909_Start
Continuous Measurement Function	Y	–	Y	–	–
Howler tone generation (very high level on analog port)	Y	2	Y	2	–
Calibration	Y	2	Y	2	–
FXS capacitance measurement	Y	2	Y	2	Is used by FXS phone detection
FXS phone detection	Y	2	Y	2	Reduces the SLIC power consumption in case no phone is currently connected. Has no effect for combined DC/DC converters.
Support for STANDBY_LP mode	Y	–	Y	–	–
FXO port	Y	–	Y	–	Requires SLC121 in combination with Clare CPC5622 and CPC5712.

Table 5 Intel® SLIC for CPE Supported Features (cont'd)

Feature	xRX200/ xRX300[1)]		GRX350[2)]/ GRX550[3)]		Restrictions/Comments
	S	C/R	S	C/R	
Miscellaneous					
Message Waiting Lamp support	Y	–	Y	–	Via tip-ring voltage change during on-hook
DC/DC Converter Types					
Inverting Buck-Boost Converter (IBB)	Y	–	Y	–	Depends on HW mounting. The application must apply a matching BBD file that is generated by XTCOS.
Combined Inverting Buck-Boost Converter (CIBB)	Y	–	Y	–	Depends on HW mounting. The application must apply a matching BBD file that is generated by XTCOS. For SLC210/SLC220 device tree configuration is needed.
Inverting Flyback Converter (IFB)	N	–	Y	–	Depends on HW mounting. Supported with SLC210/SLC220 only. The application must apply a matching BBD file that is generated by XTCOS. Requires device tree configuration.
Combined Inverting Flyback Converter (CIFB)	N	–	Y	–	Depends on HW mounting. Supported with SLC210/SLC220 only. The application must apply a matching BBD file that is generated by XTCOS. Requires device tree configuration.

1) Devices of the ARX300, xRX200, GRX300, VRX220 and ARX220 Families
2) PXB 4395 Version 1.2, PXB 4395-1600 Version 1.2, devices of the GRX350 Series
3) PXB 4583-2000 Version 1.2, device of the GRX550 Series

Table 6 Intel® Telephony Chipset for CPE DXS Series Supported Features

Feature	GRX350[1]/ GRX550[2]		Restrictions/Comments
	S	C/R	
Signaling			
Integrated DTMF generator	Y	–	–
Integrated DTMF detector	Y	–	–
Integrated FSK (Caller ID) generator, according to Bell 202 and ITU-T V.23	Y	–	–
Integrated Universal Tone Detector (UTD) to detect single frequency tones in the transmit or receive path	Y	–	The UTD is configured with BBD files generated by XTCOS
Pulse dialing detection	Y	–	–
CODEC/SLIC			
Worldwide programmability for AC transmission performance parameters (AC impedance matching, hybrid balance, transmit and receive gain, frequency response); specification in accordance with ITU-T Recommendation Q.552 for interface Z and ETSI Standard ES 202 971	Y	–	–
Integrated sinusoidal balanced and unbalanced ringing capability - programmable ringing voltage with DC offset, frequency and crest factor	Y	–	–
Loop start signaling	Y	–	–
Ground start signaling	Y	–	–
Emergency shutdown in case of overtemperature and ground fault	Y	–	–
Polarity reversal	Y	–	–
Programmable DC loop current (I_{CONST})	Y	–	DXS: 50 mA max. DXC: 32 mA max.
AC Ring Trip detection	Y	–	–
Fast Ring Trip detection	Y	–	–
Balanced ringing with DC offset	Y	–	DXS: 0..100[3] V_{RMS}/0..144[3] V_{DC} DXC: 0..70[4] V_{RMS}/0..120[4] V_{DC}
Unbalanced ringing	Y	–	DXS: 0..50 V_{RMS} DXC: 0..42 V_{RMS}
Automatic ring current regulation for power consumption reduction	Y	–	80 mA max.
DC/DC configuration for high-power ringing	Y	–	Via BBD coefficients generated by XTCOS
On-hook transmission	Y	–	–
PCM coding G.711 A-law/µ-law	Y	–	Not supported in PCM wideband mode
PCM transmission 16-bit linear	Y	–	–

Table 6 Intel® Telephony Chipset for CPE DXS Series Supported Features (cont'd)

Feature	GRX350[1]/ GRX550[2]		Restrictions/Comments
	S	C/R	
PCM interface	Y	–	–
SPI interface in 32-bit access mode	Y	–	–
SPI interface in 8-bit access mode	N	–	–
Combined Serial Interface (CSI)	N	–	–
Wideband support (16 kHz transmission)	Y	–	–
Integrated test and diagnostic functions for local-loop monitoring according to GR-909	Y	–	–
Continuous Measurement Function	Y	–	–
Open-loop calibration	Y	–	–
Capacitance measurement	Y	–	–
AC level meter	Y	–	–
Programmable 12/16 kHz teletax generation (metering)	Y	–	–
Boosted AC level for howler tone	Y	–	–
Internal device calibration	Y	–	–
Support for STANDBY mode	Y	–	–
Support for sleep condition	Y	–	–
Message Waiting Lamp support	Y	–	Not supported for combined DC/DC converter types
DC/DC Converter Types			
Inverting Buck-Boost Converter (IBB)	Y	–	–
Combined Inverting Buck-Boost Converter (CIBB)	Y	–	–
Inverting Flyback Converter (IFB)	Y	–	–
Combined Inverting Flyback Converter (CIFB)	Y	–	–

1) PXB 4395 Version 1.2, PXB 4395-1600 Version 1.2, devices of the GRX350 Series
2) PXB 4583-2000 Version 1.2, device of the GRX550 Series
3) The sum of the DC ring offset and the peak ring voltage must be smaller than 144 V
4) The sum of the DC ring offset and the peak ring voltage must be smaller than 120 V

3 Enhancements

Table 7 shows the major enhancements between the Voice System Package 4.44 RC5 and the previous version. For a full list of changes, refer to the detailed CHANGELOG file that is part of the driver package.

Table 7 Changes Since Voice System Package 4.44 RC4

Devices	Change Description for Devices Listed	Change Type
GRX350[1]**/GRX550**[2]	Support for DXS Series devices. Support of up to 4 DXS devices.	New feature
	For SLC210/SLC220 two new linefeed modes IFX_TAPI_LINE_FEED_GROUND_START_TIP_OPEN and IFX_TAPI_LINE_FEED_GROUND_START_TIP2GND were added to support ground start.	New feature
All Devices	Added field nRtpEventIntervalls to IFX_TAPI_PKT_RTP_CFG_t. This allows to change the RTP event packet transmission intervall if the FW supports this.	New feature
	Added fields bEventVolumeLimit, nEventVolMin and nEventVolMax to IFX_TAPI_PKT_RTP_CFG_t. This allows setting an upper and lower limit to the value in the volume field of RTP event packets.	New feature
	Configuring the RTP event transmission mode with IFX_TAPI_PKT_EV_OOB_ONLY now blocks the sending of RTP voice packets while RTP event packets are sent.	Improvement

1) PXB 4395 Version 1.2, PXB 4395-1600 Version 1.2, devices of the GRX350 Series

2) PXB 4583-2000 Version 1.2, device of the GRX550 Series

4 Open Issues

Table 8 contains open issues of the Voice System Package 4.44 RC5.

Table 8 Open Issues in Voice System Package 4.44 RC5

Devices	Issue Description for Devices Listed	Status
DXS102	For combined DC/DC converter designs the BBD download during the initialization sequence needs to be done in strict order of channel 0 before channel 1. Doing the BBD download in reverse order and setting linefeed before the BBD download on channel 0 can lead to damage to the switching transistor of the DC/DC converter. **Workaround:** Ensure that the BBD download is done on channel 0 then channel 1 before setting linefeed on any of the lines.	Open
xRX200/ xRX300[1)]	When announcement is started without automatic loop, the announcement ends after one playout and the announcement end event is received. Starting the announcement again will produce an error indicating that the announcement is still being played, which is not true. **Workaround:** Call IFX_TAPI_COD_ANNOUNCE_STOP after receiving the event IFX_TAPI_EVENT_COD_ANNOUNCE_END to allow replay of the announcement.	Open
All Devices	In between simple tones an inaudible pause of 2-3 ms occurs	Open
All Devices	On UGW 7.1 TAPIDEMO fails to retrieve the DECT RF parameters	Open
DXS101/DXS102 at GRX350/GRX550	T.38 FAX transparent mode does not work on FXS ports of the DXS Series devices when tested with TAPIDEMO	Open

1) Devices of the ARX300, XWAY™ xRX200, GRX300, VRX220 and ARX220 Families

5 RTCP-XR Support

RTCP-XR according to RFC 3611 is supported.

Not all items defined in RFC 3611 are supported, because a full implementation increases the memory requirements and the complexity of the voice subsystem without being of real practical use. For instance the run-length encoded statistics are not included because of this reason.

The voice subsystem does not generate autonomously RTCP-XR packets. Instead the application can request the supported metrics, pack them into a UDP packet and forward them to the recipient. The metrics are provided by the VoIP Subsystem in the format defined in RFC 3611, so the application does not need to reformat them. For unsupported fields the code for “unavailable” defined in RFC 3611 for the respective field is set.

The report blocks given in **Table 9** are supported:

Table 9 Supported RFC 3611 Report Blocks

Chapter in RFC 3611	Field	Support
4.6. Statistics Summary Report Block	BT	supported, Block Type, BT = 6
	L	supported, Loss Report Flag, L = 1
	D	supported, Duplicate Report Flag, D = 1
	J	supported, Jitter Report Flag, J = 1
	ToH	not supported
	block length	supported, block length = 9
	SSRC source	supported
	begin seq	supported
	lost packets	supported
	dup packets	supported
	min jitter	supported
	max jitter	supported
	mean jitter	supported
	dev jitter	supported
	min ttl hl	not supported
	max ttl hl	not supported
	mean ttl or hl	not supported
	dev ttl or hl	not supported

Table 9 Supported RFC 3611 Report Blocks

Chapter in RFC 3611	Field	Support
4.7. VoIP Metrics Report Block	BT	supported, BT = 7
	SSRC source	supported
	loss rate	supported
	discard rate	supported
	burst density	supported
	gap density	supported
	burst duration	not supported
	gap duration	not supported
	round trip delay	not supported
	end system delay	supported
	signal level	supported
	noise level	supported
	RERL	supported
	Gmin	supported, set to 16
	R factor	not supported
	ext R factor	not supported
	MOS-LQ	not supported
	MOS-CQ	not supported
	RX config	not supported
	JB nominal	not supported
	JB maximum	not supported
	JB abs max	not supported
	burst number*	supported

6 Device Tree Configuration

To adapt the driver to different hardware configuration the Linux* device tree is supported by the drivers. Five of the drivers look in the device tree for configuration:

1. The drv_vmmc driver which is used for xRX200 and xRX300 family devices, looks for the details of the MPS block.
2. The drv_vmmc_xrx500 driver which is used only for GRX350/GRX550 series devices, looks for the details of the MPS block.
3. The drv_sdd_mbx driver which is used only for GRX350/GRX550 series devices, looks for the details of the VCODEC as a SPI client, as well as for the details of the Intel® SLIC for CPE SLC210/SLC220 devices.
4. The DXS Series driver is used only in conjunction with GRX350/GRX550 series devices. It is a SPI bus platform device and looks for details of the DXS Series devices as a SPI client.
5. The board driver which is only suitable for Intel evaluation board “GRX500 EVM” to which an EASY 32002 EXT board with DXS Series device is attached. It controls the extension board and looks for details how to act as an SPI proxy in between the GRX350/GRX550 and the DXS. The driver is given to customers as an example how to implement a board driver supporting multiple DXS devices.

6.1 Device Tree Information for drv_vmmc Driver

This device tree information is valid for the drv_vmmc driver.

drv_vmmc Driver

Node describing MPS register block

Required properties:

- compatible: must be equal to "lantiq,mps-xrx100"
- reg: address and range of the MPS register block
- interrupts: interrupt numbers associated with the MPS AD0 and AD1 registers
- interrupt-parent: reference to the icu
- lantiq,mps: reference to node describing the MPS mailbox SRAM

Optional properties:

- none

Node describing MPS mailbox SRAM

Required properties:

- reg: address and range of the MPS mailbox SRAM

Optional properties:

- none

Example:

```
mps@107000 {
        compatible = "lantiq,mps-xrx100";
        reg = <0x107000 0x400>;
        interrupt-parent = <&icu0>;
        interrupts = <154 155>;
        lantiq,mbx = <&mpsmbx>;
};
mpsmbx: mpsmbx@200000 {
        reg = <0x200000 0x200>;
};
```

6.2 Device Tree Information for drv_vmmc_xrx500 Driver

This device tree information is valid for the VMMC xRX500 driver since version 1.20.1.0.

drv_vmmc_xrx500 Driver

Node describing MPS register block

Required properties:

- compatible: must be equal to "lantiq,xrx500-mps"
- reg: address and range of the MPS register block
- interrupts: interrupt numbers associated with the MPS AD0 and AD1 registers
- interrupt-parent: reference to the gic
- lantiq,mps: reference to node describing the MPS mailbox SRAM
- pinctrl-names: must be equal to "pcm"
- pinctrl-0: reference to pin control defining how and which pins to use for PCM (TDM).

Optional properties:

- none

Node describing MPS mailbox SRAM

Required properties:

- reg: address and range of the MPS mailbox SRAM

Optional properties:

- none

Example:

```
        mps@1107000 {
                compatible = "lantiq,xrx500-mps";
                reg = <0x1107000 0x400>;
                interrupt-parent = <&gic>;
                interrupts = <154 155>;
                lantiq,mbx = <&mpsmbx>;
                pinctrl-names = "pcm";
                pinctrl-0 = <&pinctrl_tdm>;
        };

        mpsmbx: mpsmbx@1200000 {
                reg = <0x1200000 0x200>;
        };
```

6.3 Device Tree Information for drv_sdd_mbx Driver

The drv_sdd_mbx driver provides access to the VCODEC.

drv_sdd_mbx Driver

To describe the VCODEC use the following nodes in the device tree:

Required Properties:

- compatible: must be equal to "lantiq,grx500-vcodec"
- reg: SPI chip select line number to which the VCODEC is attached.
- interrupts: interrupt number to which the VCODEC is attached.
- interrupt-parent: reference to the gic
- slic child node if a SLC210/SLC220 (previous name: SLIC 200 family or SLIC 210/220) device is used with these properties:
  - compatible: must be equal to "lantiq,slic200"
  - dcdc_type: String from below list describing the DC/DC converter type used:

    IBB

    CIBB

    IFB

    CIFB

Optional Properties:

- SPI-max-frequency: the SPI frequency used to access the VCODEC, may not exceed 8 MHz

Example:

```
vcodec@5 {
        compatible = "lantiq,grx500-vcodec";
        spi-max-frequency = <8000000>;
        reg = <5>;
        interrupts = <217>;
        interrupt-parent = <&gic>;

        slic200@0 {
                compatible = "lantiq,slic200";
                dcdc_type = "IBB";
        };
};
```

6.4 Device Tree Information for DXS Driver

This device tree information is valid for the DXS driver since version 1.1.0.0.

DXS Driver

Node describing DXS Series platform SPI device

Required properties:

- compatible: must be equal to "lantiq,duslicxs"
- reg: SPI chip select line number to which the DXS device is attached.
- spi-max-frequency: the maximum SPI frequency used by the master, limit to 2 MHz
- spi-cpha: required to set SPI mode 3
- spi-cpol: required to set SPI mode 3
- interrupts: interrupt number the DXS device is attached to (reserved for use in the next version, not used in this version)
- interrupt-parent: reference to the gic (reserved for use in the next version, not used in this version)

Optional properties:

- none

Example:

```
        duslicxs@1 {
                compatible = "lantiq,duslicxs";
                reg = <1>;
                spi-max-frequency = <2000000>;
                spi-cpha;
                spi-cpol;
                interrupts = <280>;
                interrupt-parent = <&gic>;
        };
```

6.5 Device Tree Information for Board Driver

This device tree information is valid for the board driver compiled for GRX500 EVM with EASY 32002 EXT since version 1.2.0.0.

Board Driver

Node describing the board driver as a platform SPI device.

Required properties:

- compatible: Must be equal to "lantiq,easy32002_ext".
- reg: SPI chip select line number at GRX350/GRX550.
- reset-gpios: Reset line for all devices on the extension board.
- address-gpios: Address lines to select a device.
- dcdchw-gpios: DC\DC type of all DXS devices.
- brdrd-gpios: Read selected (with address lines) DC\DC type for one DXS device.
- brddt-gpios: Board detection GPIO. The extension board pulls line down when connected.
- spi-max-frequency: the maximum SPI frequency used by the master, limit to 2 MHz.
- spi-cpha: required to set SPI mode 3.
- spi-cpol: required to set SPI mode 3.
- as child nodes add DXS driver blocks where reg addresses the slot on the EASY 32002 EXT board and ranges from 0 to 3.

Optional properties:

- none

Example:

```
easy32002_ext@1 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <1>;
        compatible = "lantiq,easy32002_ext";
        reset-gpio = <&gpio0 1 0>;
        address-gpios = <&gpio0 11 0>, <&gpio0 14 0>, <&gpio0 21 0>;
      dcdchw-gpios = <&gpio1 0 0>, <&gpio1 1 0>, <&gpio1 10 0>, <&gpio1 11 0>;
        brdrd-gpio = <&gpio0 19 0>;
        brddt-gpio = <&gpio0 10 0>;

        spi-max-frequency = <2000000>;
        spi-cpha;
        spi-cpol;

        duslicxs@0 {
                compatible = "lantiq,duslicxs";
                reg = <0>;
                spi-max-frequency = <2000000>;
                spi-cpha;
                spi-cpol;
                interrupts = <280>;
                interrupt-parent = <&gic>;
```

```
        };

        duslicxs@1 {
                compatible = "lantiq,duslicxs";
                reg = <1>;
                spi-max-frequency = <2000000>;
                spi-cpha;
                spi-cpol;
                interrupts = <280>;
                interrupt-parent = <&gic>;
        };

        duslicxs@2 {
                compatible = "lantiq,duslicxs";
                reg = <2>;
                spi-max-frequency = <2000000>;
                spi-cpha;
                spi-cpol;
                interrupts = <280>;
                interrupt-parent = <&gic>;
        };

        duslicxs@3 {
                compatible = "lantiq,duslicxs";
                reg = <3>;
                spi-max-frequency = <2000000>;
                spi-cpha;
                spi-cpol;
                interrupts = <280>;
                interrupt-parent = <&gic>;
        };
};
```

Literature References

[1] CPE Gateway SoCs Voice over IP and POTS System User's Manual System Description Rev. 2.0, 2012-03-15

[2] Gateway SoCs/SLC220/SLC210 FXS Line Interface User's Manual System Description Rev. 1.0, 2016-09-15

[3] Gateway SoCs Voice Processing User's Manual System Description Rev. 3.0, 2016-09-30

[4] DXS User's Manual System Description Rev. 2.1, 2016-02-19

[5] ARX388 VoIP Firmware 2.1.0.8.0 Release Note Rev. 1.0, 2015-07-24

[6] GRX288/VRX288 VoIP Firmware 3.5.0.7.0 Release Note Rev. 1.0, 2015-07-24

[7] XTCOS Software V4.4.0.0 Release Note Rev. 1.0, 2015-10-23

[8] EASY 350 VDSL over POTS Reference Board Getting Started Rev. 1.2, 2016-06-08

Attention: Please refer to the latest revision of the documents.