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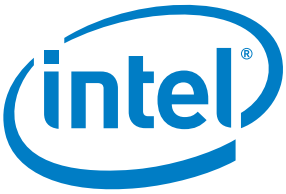

# Intel® Telephony Chipset for CPE

DXS Series

DXS102 (PEF32002VTV11)
DXS102 (PEF32002VTV12)
DXS101 (PEF32001VV11)
DXS101 (PEF32001VTV12, PEF32001VV12, PEF32001VSV12)

# User's Manual

System Description

Revision 2.2, 2017-05-30 Intel
Confidential
Reference ID 617585

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**Revision History**

| | |
|---|---|
| **Current:** | **Revision 2.2, 2017-05-30** |
| **Previous:** | **Revision 2.1, 2016-02-19** |

| Page | Major changes since previous revision |
|---|---|
| All | The products described in this document have been rebranded with new ordering codes and names, amongst others the following have been changed:<br>• "DUSLIC™ XS Family" renamed "Intel® Telephony Chipset for CPE, DXS Series"<br>• DUSLIC™ XS2 renamed DXS102<br>• DUSLIC™ XS1 renamed DXS101 |
| **35** | **Chapter 2.2.10 Hook Detection in STANDBY Mode** updated. |
| **42** | **Chapter 2.2.17 Combined DC/DC Converter** updated as follows:<br>• Limitation removed: "Line testing / calibration is only allowed if the other channel is DISABLED". |
| **52** | **Chapter 2.4.1.1 Standard GR-909 Tests** updated as follows:<br>• Footnote removed: "In the case of a combined DC/DC converter, GR909 can only be executed if the neighboring channel is in DISABLED mode".<br>• Minor text improvements.<br>• Further information added to Footnote 1 of **Table 8**.<br>• Text and **Figure 32** updated to make required setting of modes clearer. |
| **55** | **Chapter 2.4.1.2 Capacitance Measurement** updated to make required setting of modes clearer. |
| **57** | **Chapter 2.4.2 Open Loop Calibration (OLC)**: Section on "Line Testing with Default OLC Values" and **Figure 34** made clearer, added description for open loop calibration values. |
| **61** | **Chapter 2.4.4 AC Level Meter** updated to make required setting of modes clearer. |
| **69** | **Literature References** updated. |

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# Preface

This User's Manual System Description describes the system features and performance characteristics of the DXS system. This includes:

- DXS102 or DXS101 devices.
- The firmware and software associated with the DXS system.

This User's Manual is part of the DXS Series documentation package. Further DXS Series related documents are available via your local Intel sales team or can be downloaded from the customer portal on the Intel website.

To simplify matters, the following synonyms are used:

**DXS, DXS Series**

Synonym used for the following devices:

- DXS102 (PEF32002VTV11, PEF32002VTV12)
- DXS101 (PEF32001VV11, PEF32001VTV12, PEF32001VV12, PEF32001VSV12)

**SLIC**

Synonym used for the SLIC-part of the DXS102/DXS101 device.

For detailed information about DXS Series devices, please refer to the related data sheets **[2]**, **[3]**, **[4]**.

**Organization of this Document**

This document is organized as follows:

- **Chapter 1**, **Introduction**
  An introduction to the DXS system including key features, typical applications and an overview of the available documentation.
- **Chapter 2**, **Functional Description**
  Description of POTS functionality (BORSCHT functions, supply and external components), voice/data processing (resource management, Caller ID and fax/modem support) and control firmware (host interface communication, resources, submodule description).
- **Chapter 3**, **Device Driver and API Functions**
  A summary of the available API function calls.
- **Literature References** and **Standards References**

# 1 Introduction

The Intel® Telephony Chipset for CPE DXS Series is Intel's solution for next generation analog voice and VoIP linecards, IP Private Branch Exchanges (PBXes) and a variety of similar applications. DXS Series devices provide all the features required for analog line processing and the interface to the POTS line. The devices exchange voice data between analog lines (traditional POTS lines) and the PCM highway, generate or detect special signaling (DTMF, Metering, Ringing, etc) as well as provide enhanced line testing and self-testing features.

## 1.1 System Overview

**Figure 1** shows the system architecture where the DXS Series device is controlled using the DXS API Library.

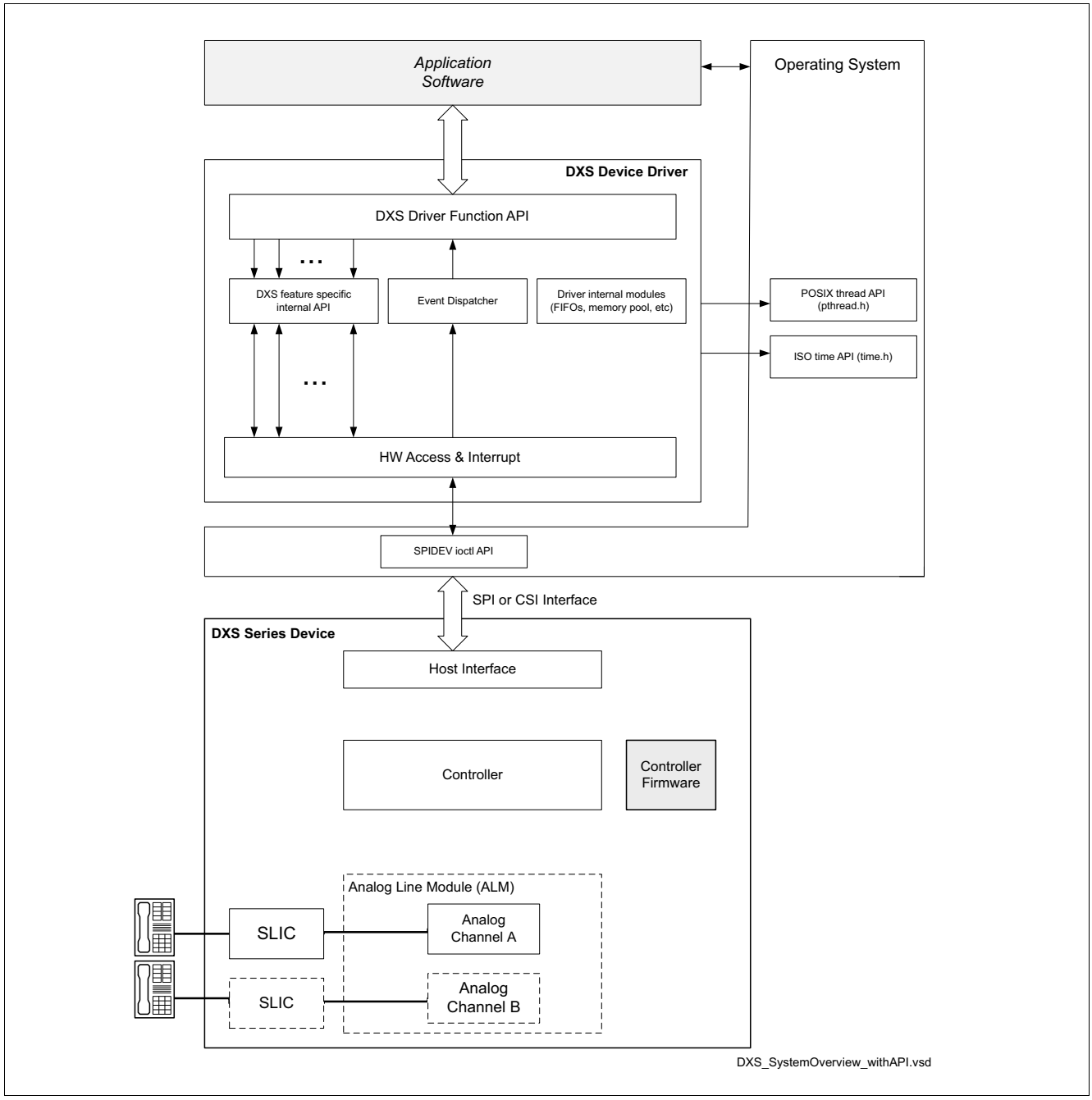


**Figure 1 DXS System Overview**

The DXS system package includes the following components:

- DXS Series devices
- DXS Driver Package, including a DXS Device Driver and the DXS Application Programming Interface (API) used to control the telephony functionality (see **Chapter 3**)
- XTCOS coefficient calculation software
- DXS Series documentation (see **Chapter 1.3**)
- DXS firmware

## 1.2 Typical Applications

Typical applications that use the DXS system package are:

- Residential VoIP Router / Gateway
- Analog Telephone Adapter (ATA)
- Integrated Access Device (IAD)
- xPON
- Cable Modem, embedded Media Terminal Adaptor (eMTAs), Standalone Media Terminal Adaptor (SMTAs)
- PBX
- ISDN CPE, xDSL CPE

A typical application using the DXS system is shown in **Figure 2**.

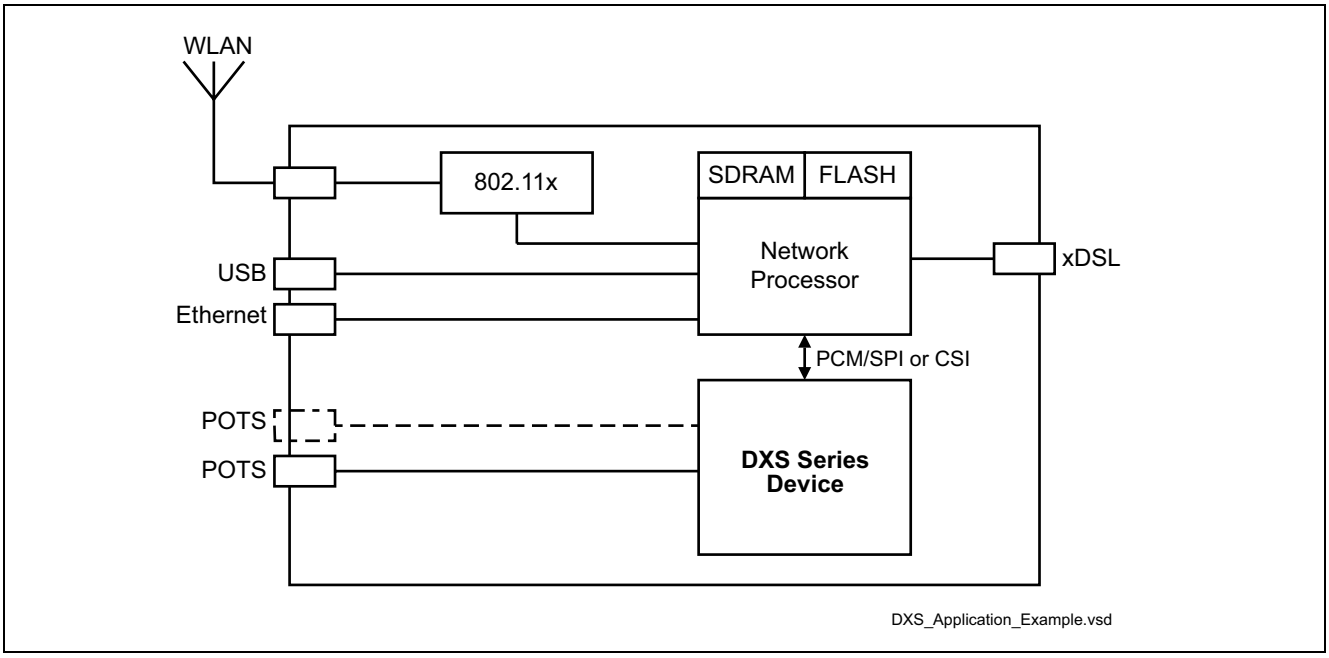


**Figure 2 Application Example: ATA / VOIP Router / Wireless Router**

## 1.3 User Documentation

The DXS system is provided with the user documentation listed in **Table 1**:

**Table 1 Documentation Structure**

| Component | Document | Document Content |
|---|---|---|
| **Hardware Documents** | | |
| DXS102<br>DXS101 | Product Brief [1] | An overview of product features, tools and applications. |
| | Data Sheet<br>[2], [3], [4] | The data sheet provides information on all the hardware information necessary for application design: pin layout, pin description, clocking, reset behavior, interfaces, application circuits, package outlines, Bill of Materials. It contains detailed design guidelines, information on concepts of power and ground planes and layout guidelines. It also covers the electrical characteristics and transmission performance and a standards reference. |
| **Software Documents** | | |
| DXS API,<br>DXS Device Driver | User's Manual<br>Programmer's Reference [5] | This document describes the DXS programming functions and their use. |
| **System Documents** | | |
| DXS System | User's Manual<br>System Description | The system description provides information on the system functions and characteristics of the DXS system. It gives an overview of the system and components. |
| DXS System Package | Release Note [6] | Release notes for the DXS System Package containing detailed lists of components, supported features, changes and known issues. |
| **Tooling Documents** | | |
| EASY 3200x/3100x Evaluation Package | Tool Brief [7] | A two-page overview describing typical applications and the hardware and software features of the evaluation boards and the complete package. |
| | Getting Started [8] | This document describes the components of the Evaluation Package. It describes the functional blocks of the reference boards, and provides details on how to operate the boards, as well as using or updating the available software.<br>It describes how to use the command line interface (CLI), how to use the XTCOS software and explains the measurement setup with PCM-4. |
| | Latest Information [9] | This document describes the hardware and software components of the Evaluation Package and provides further information about known restrictions or open issues.<br>It also describes how to get the latest documentation and software from the Intel customer portal and how to update to the latest software. |
| DXS Controller Board / Reference Boards | User's Manual<br>Hardware Description<br>[10], [11] | These documents describe the basic structure and features of the BASE board and the reference boards. They provide information on the board interfaces, a block diagram, as well as pinouts of the headers / connectors, board control and configuration. |

**Table 1 Documentation Structure** (cont'd)

| Component | Document | Document Content |
|---|---|---|
| **Further Documentation** | | |
| DXS DC/DC Converter | Application Note [12] | This document provides basic information about DC/DC converters and is a guide for the design of the external circuitry. The document describes different application circuits and their topologies as recommended by Intel. Additionally, it deals with layout considerations and hints for placement and routing of components on the PCB. |
| DXS Protection against Surge and Power Faults | Application Note [13], [14] | This document provides information about protecting DXS Series devices against lightning and AC power-fault conditions according to ITU-T K.21 and Telcordia GR-1089-CORE requirements. It consists of major chapters describing: protection recommendations for non-isolated equipment; protection recommendations for isolated equipment; and detection of fault conditions. |

The latest revision of the DXS Series related user documentation listed above is available from your local Intel sales team or via the Customer Portal on the Intel website.

# 2 Functional Description

## 2.1 Block Diagram

**Figure 3** depicts the internal structure of the DXS Series device. The main blocks are:

- Analog Line Module (ALM) supporting one or two analog line channels (channel A and B). The analog line channels provide the interface to the internal SLIC devices.
- PWM controller per DC/DC converter to support SLIC supply voltage generation.
- Controller with internal ROM and RAM. Used for signaling and control.
- General Purpose IOs (GPIOs)
- PCM interface
- Serial Peripheral Interface (SPI) with corresponding interrupt lines
- Combined Serial Interface (CSI) - alternative to PCM and SPI interface

The analog line channels, controller and host interfaces exchange data via an internal BUS and are synchronized via the PLL clock control.

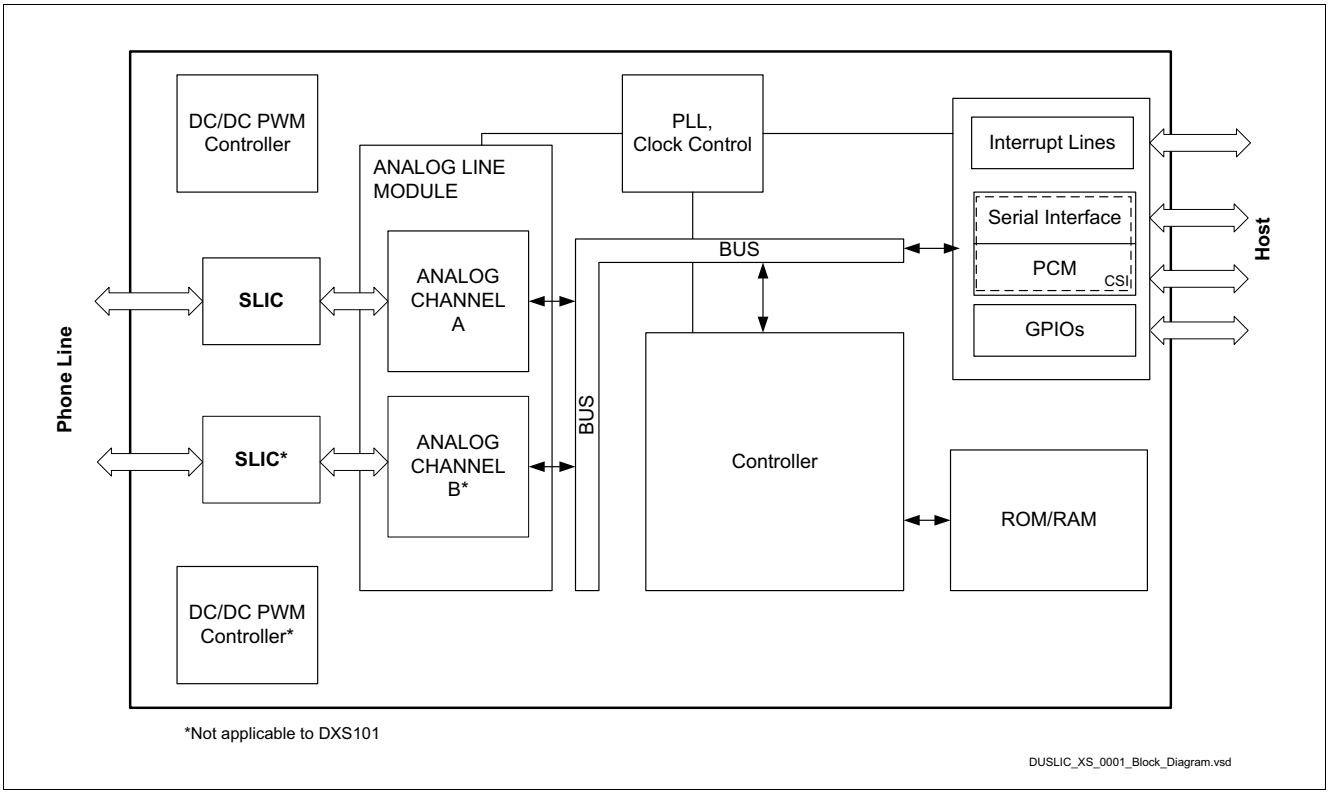


**Figure 3 Block Diagram of DXS Series Device**

### Subscriber Line Interface Circuit (SLIC)

A SLIC applies high voltages to the line to provide a DC line feeding or ringing signal. It adds the AC voice signal from the analog line module to the line and measures the line current.

### Analog Line Module (ALM)

The ALM receives the measured line current and performs an analog-to-digital conversion. The digital signals are further processed and passed on to the controller. Conversely, the ALM receives digital signals from the controller and performs a digital to analog conversion, providing analog signals for the SLIC(s). Details of the ALM are shown in **Figure 7**.

### Controller

The controller is the main part of the DXS. It is responsible for handling the host interface communication, the PCM interface and the GPIOs. It also controls the ALM, the DC/DC PWM controllers and the SLICs. In addition, it performs some voice processing, A-law and µ-law (G.711) companding, as well as tone generation and detection.

The firmware for booting and basic operation is located in the on-chip ROM. Extensions for this ROM-based firmware can be downloaded into the on-chip RAM. It is essential to download the latest firmware provided in the system package in order to ensure that the device behaves correctly.

### PWM Controller for DC/DC Converter

The SLIC requires a high supply voltage, which is negative with respect to ground. The level of the required supply voltage depends on the operating mode of the line. Therefore, the SLIC supply voltage is generated by an external DC/DC converter, where the pulse width modulator (PWM) controller is located inside the DXS. The PWM controller can be configured to adapt to different output voltage and power requirements and to control different DC/DC converter topologies. Further details can be found in **Chapter 2.2.16**.

### Serial Peripheral Interface (SPI)

The SPI interface is the control interface between the external host controller and the on-chip controller of the DXS. The interface contains two internal mailboxes - one for commands in the downstream direction, and one for command responses and events in the upstream direction, see **Figure 4**.

Data transferred from the host to the DXS device is written to the In-Box. Data in the upstream direction could be the answer to a command message or an unsolicited event message (for example, in the case of a hook-change event). This data is stored in the Out-Box of the DXS (combined command and event box). If configured, an interrupt is generated in order to signal to the host that there is data ready to be read. Alternatively, the host can poll the host interface. The host interface also contains hardware registers for interface handshaking and status information. The handshake registers are handled directly by the DXS Device Driver during boot and firmware download. The status information is directly processed by the driver and mapped to its variables.

The serial peripheral interface (SPI) is compatible with the Motorola SPI and the Intel SCI. It is built as a serial slave interface supporting Motorola SPI mode 3. Finally, the SPI interface provides 32/16-bit access support.

### PCM Interface

The PCM Interface Module of the DXS device supports up to two PCM channels. Each PCM channel can be activated separately via the associated phone channel. Typically, 8 kHz 8-bit compressed voice data (A-/µ-law) is transmitted via the PCM interface, but alternatively 16-bit linear data can be configured.

In addition, the DXS supports two wideband modes. One wideband mode uses four consecutive time slots (32-bit), where the first 16-bit word is the first 16 kHz sample, and the second 16-bit word is the second 16 kHz sample. The other wideband mode provides 16 kHz sampling with 16 kHz spacing. This means that there is no change for the first 16-bit word, but the second 16-bit word is provided 62.5 µs after the first 16-bit word. Both wideband modes only support linear coding.

### Combined Serial Interface (CSI)

The Intel CSI allows the transmission of control data and voice data via a single serial interface. Internally, the data stream from the CSI interface is again split up for separate PCM and control interfaces, see **Figure 3** and **Figure 4**.

The advantage of CSI compared to PCM and SPI is that fewer signals have to be connected to the DXS. Especially in the case of large SoCs, it is an advantage to integrate a CSI master module to save pin count at the SoC. A further advantage is that it is much cheaper to galvanically isolate the DXS because only 4 signal lines need to be isolated.

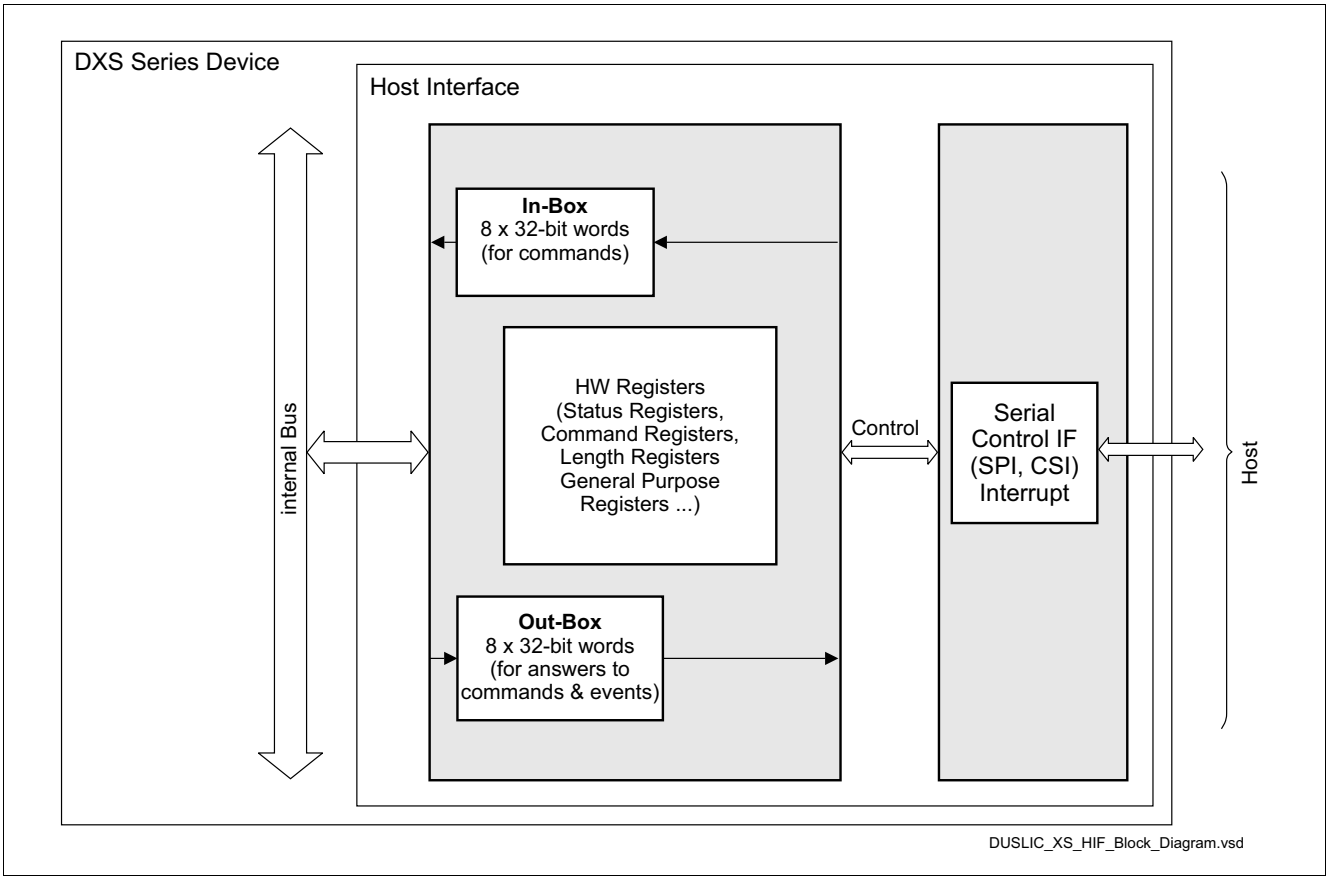


**Figure 4 Block Diagram of DXS Interfaces**

## 2.2 POTS Features

### 2.2.1 BORSCHT Functions

The following BORSCHT functions are supported by the DXS:

- **Battery Feed**
  The DXS offers a DC battery feed characteristic with a constant current and a constant voltage region (see **Figure 6**).
- **Overvoltage Protection**
  Overvoltage protection is indispensable in preventing damage to the line circuit in cases where the system is exposed to high voltages resulting from power lines crossing or lightning.
  The robust high-voltage SLIC technology, together with the external low cost protection circuit, forms a reliable overvoltage protection solution for the SLIC against overvoltages from the tip and ring lines.
- **Ringing**
  The ringing signal is a low-frequency, high-voltage signal sent to the subscriber equipment to ring the telephone. The ringing signal is generated by the DXS, which supports quasi-balanced ringing – the most power effective method of ring signal generation.
- **Signaling**
  The main signaling method is loop start signaling, in which the start of the call is initiated by closing the subscriber loop (phone goes off-hook). The hook information is also part of pulse dial signaling, where the number of hook pulses indicates the telephone number to be called. Besides these, other signaling methods supported by the DXS are DTMF signaling, ground start signaling, battery reverse signaling, and TTX (Metering) signaling.
- **Hybrid for 2/4-wire Conversion**
  The subscriber equipment is connected to a 2-wire interface (tip and ring) where the information is transmitted bidirectionally. For digital transmission via the switching network, the information must be split into separate transmit and receive paths (4 wires). To avoid generating echoes, the hybrid function requires a balanced network matched to the line impedance. Hybrid balancing can be programmed in the DXS device without changing any external components.
- **Testing**
  The DXS offers line-testing functionality as described in **Chapter 2.4**, including GR-909 testing, capacitance measurement, and AC level measurements for voice transmission quality self-testing.

### 2.2.2 Programmability

Conventional designs require a large number of external components to adapt the circuit for use in different countries and applications. The digital signal processing of the DXS allows for the following parameters to be modified by updating the coefficients that control the DSP algorithms for the analog line module.

- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid
- Frequency response in transmit and receive direction
- Ringing frequency and amplitude
- Ring trip threshold
- On/off-hook detection threshold
- DC line current and voltage

A complete set of parameters is entered into the XTCOS tool and used to calculate the coefficients. These coefficients are provided to the device driver as a coefficient file.

This means that, for example, changing the input impedance requires no hardware modifications. Instead, a subset of coefficients can be downloaded. A single piece of hardware is now capable of meeting the requirements for different markets. The digital nature of the filters and gain stages assures high reliability, no drift (across temperature or time) and minimal variations between different lines.

Each analog channel can be programmed independently of the other channels. XTCOS allows for the generation of the coefficient set required to match a given standard requirement.

### 2.2.3 AC and DC Settings

Table 2 shows the programmable settings for the DXS AC and DC characteristics, including the default values of these settings.

**Table 2 Programmable Settings (Default, Min, Max)**

| Name | Default | Min. | Max. | Unit |
|---|---|---|---|---|
| **AC** | | | | |
| AC Characteristic | 600 | – | – | Ω |
| Relative Level TX | 3 | -4 | – | dB |
| Relative Level RX | -10 | – | 0.5[1)] | dB |
| **DC** | | | | |
| Constant Voltage | 40 | 0 | 72 | V |
| Constant Current | 20 | 0 | 50 | mA |
| Active DUP Time (hook debouncing in ACTIVE mode) | 13 | 2 | 16 | ms |
| Ground Key DUP Time (ground key detection debouncing time) | 52 | 4 | 60 | ms |
| Emergency Shutdown (ESD) DUP Time | 10 | 6 | 15 | ms |
| Hook Threshold (ACTIVE mode, off-hook → on-hook) | 8 | 0 | 50 | mA |
| Hook Threshold (ACTIVE mode, on-hook → off-hook) | 10 | 0 | 50 | mA |
| DC Regulation Speed Parameter | 1 | 0 | 1 | – |
| DC/DC Converter Overhead Voltage | 7 | 5 | 12 | V |
| Message Waiting[2)] Lamp Voltage | 100 | 0 | 144 | V |
| Message Waiting Hook Threshold | 15 | 0 | 50 | mA |
| Message Waiting Slope | 200 | 100 | 1000 | V/s |
| Message Waiting Cadence On Time | 1000 | 0 | 6375 | ms |
| Message Waiting Cadence Off Time | 1000 | 0 | 6375 | ms |
| **Ground Start** | | | | |
| Ground Start DUP Time (hook debouncing during ground start) | 13 | 2 | 16 | ms |
| **Ringing** | | | | |
| Ring Trip Type | DC Ring Trip | | | |
| Ring Trip Threshold | 3 | 0 | 80 | mA |
| Ringing Signal | Sinusoidal | – | – | – |
| Crest Factor | 1.42 | 1 | 1.73 | – |
| Ringing Frequency | 25 | 15 | 50 | Hz |

**Table 2 Programmable Settings (Default, Min, Max)** (cont'd)

| Name | Default | Min. | Max. | Unit |
|---|---|---|---|---|
| Ringing Amplitude | 45 | 0 | 100[3)] | $V_{RMS}$ |
| Ringing DC Offset | 12 | 0 | 144[3)] | V |
| Maximum Ring Current (for ring current regulation) | 40 | 0 | 80 | mA |
| Minimum Ring Voltage (for ring current regulation) | 45 | 0 | 100[3)] | $V_{RMS}$ |
| **TTX (Metering)** | | | | |
| TTX Frequency | 12 | 12 | 16 | kHz |
| TTX Amplitude | 0.2 | 0 | 1[4)] | $V_{RMS}$ |
| TTX Burst Length | 0 | 0 | 32767 | ms |
| TTX Slope Time | 2 | 0 | 16 | ms |
| TTX Termination Impedance[5)] R1 | 220 | 0 | 10000 | Ω |
| TTX Termination Impedance R2 | 0 | – | – | Ω |
| TTX Termination Impedance C | 0 | – | 5 | µF |

1) Programmable RX range by means of the **DxsGainsSet** function. XTCOS allows for the calculation of RX relative levels greater than 0.5 dB, up to +3 dB. However, when using a BBD file with RX relative level greater than 0.5 dBr, the use of **DxsGainsSet** will lead to incorrect levels.
2) Message Waiting Indication with glow lamp (MWL), see **Chapter 2.2.13**
3) The sum of the DC ring offset and the ring voltage must be smaller than 144 V.
4) 1 $V_{RMS}$ possible with some restrictions, see **Chapter 2.2.17.1**. XTCOS generates a warning if the desired amplitude cannot be generated over the specified TTX Termination Impedance.
5) XTCOS allows the calculation of the TTX Amplitude at a specific TTX Termination Impedance, which can be defined by means of three parameters R1, R2 and C. The TTX Termination Impedance must be within the limits of the AC impedance (see **Figure 8**).

### 2.2.4 Operating Modes

The supported DXS channel-specific operating modes are shown in **Figure 5**. Solid red lines mark the transitions that are initiated by the chip firmware (automatic transition). Dashed black lines mark transitions that must be initiated by software commands. A description of the operating modes is given in **Table 4**.

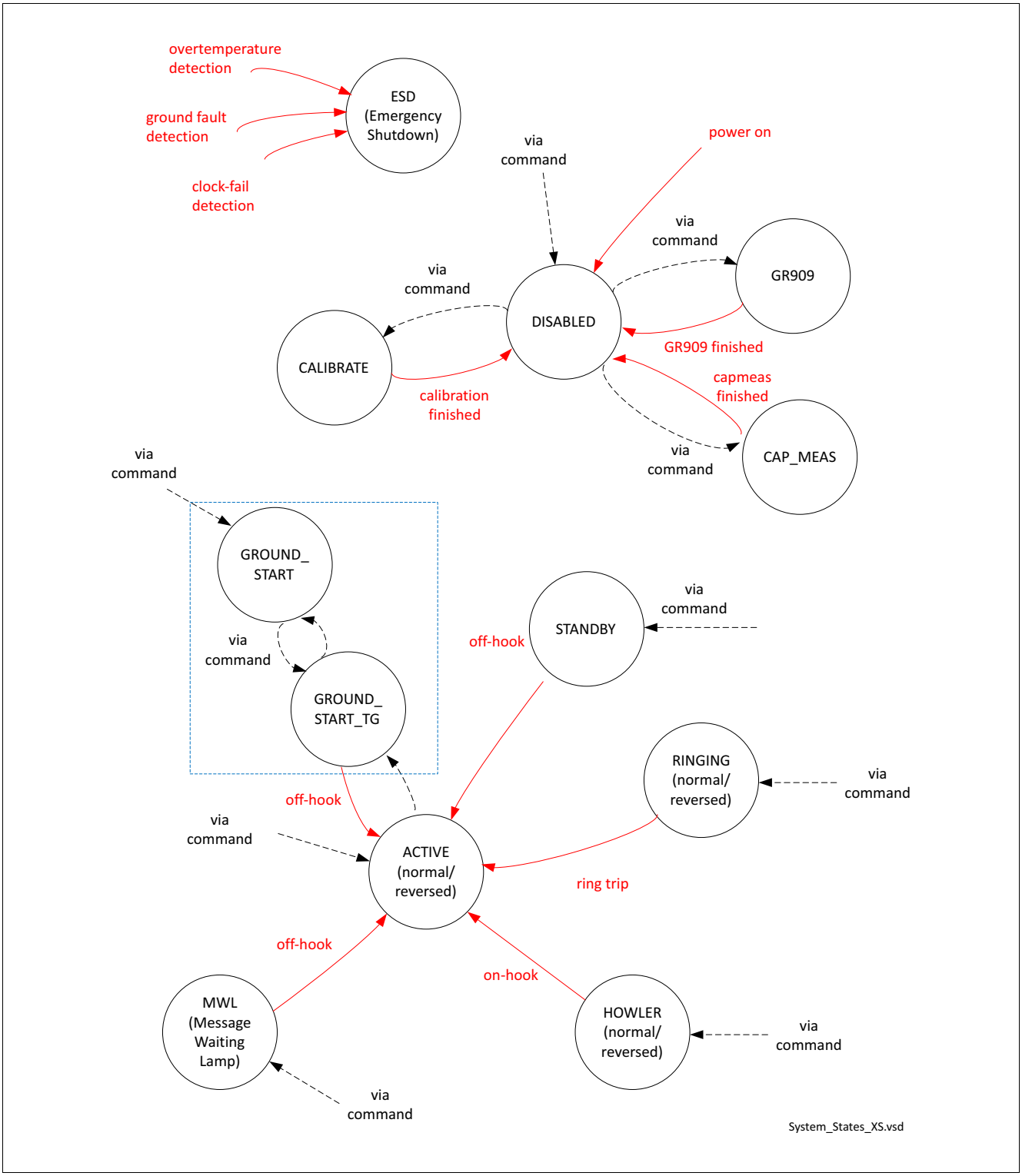


**Figure 5 DXS System Modes**

**Table 3 Operating Mode Description**

| System State | Description | Transition |
|---|---|---|
| DISABLED | No voltage is supplied to tip or ring.<br>No hook detection.<br>DC/DC converter is switched off.<br>DISABLED mode can be entered from any operating mode with immediate effect. | **Automatically entered:**<br>• Chip reset<br>• End of line testing<br>• End of calibration<br>**Allowed operating modes:**<br>• STANDBY<br>• ACTIVE / ACTIVE_REVPOL<br>• RINGING / RINGING_REVPOL<br>• GROUND_START<br>• CALIBRATION<br>• GR909<br>• CAP_MEAS |
| STANDBY | Low power mode.<br>DC feeding is active and hook detection is active.<br>No AC transmission is possible.<br>Overtemperature detection and clock-fail detection is active. | **Automatic transition to:**<br>• ACTIVE in case of off-hook<br>**Allowed operating modes:**<br>• DISABLED<br>• ACTIVE / ACTIVE_REVPOL<br>• RINGING / RINGING_REVPOL |
| ACTIVE | Voice transmission and hook detection is active.<br>Ground fault, overtemperature and clock-fail detection is active.<br>DC line feeding with programmed DC characteristic.<br>Tone generation and detection is possible. | **Allowed operating modes in on-hook:**<br>• DISABLED<br>• STANDBY<br>• ACTIVE_REVPOL<br>• RINGING<br>• GOUND_START<br>• ACTIVE_MWL<br>**Allowed operating modes in off-hook:**<br>• DISABLED<br>• ACTIVE_REVPOL<br>• ACTIVE_HOWL |
| ACTIVE_REVPOL | Voice transmission and hook detection is active.<br>Ground fault, overtemperature and clock-fail detection is active.<br>DC line feeding with programmed DC characteristic.<br>Tone generation and detection is possible. | **Allowed operating modes in on-hook:**<br>• DISABLED<br>• STANDBY<br>• ACTIVE<br>• RINGING_REVPOL<br>• GOUND_START<br>**Allowed operating modes in off-hook:**<br>• DISABLED<br>• ACTIVE<br>• ACTIVE_HOWL_REVPOL |
| RINGING | Output of ring signal to telephone line with programmed frequency and amplitude.<br>Ground fault, overtemperature and clock-fail detection is possible. | **Automatic transition to:**<br>• ACTIVE in case of ring trip<br>**Allowed operating modes:**<br>• DISABLED<br>• STANDBY<br>• ACTIVE<br>• GOUND_START |

**Table 3 Operating Mode Description** (cont'd)

| System State | Description | Transition |
|---|---|---|
| RINGING_REVPOL | Output of ring signal to telephone line with programmed frequency and amplitude.<br>Ground fault, overtemperature and clock-fail detection is possible. | **Automatic transition to:**<br>• ACTIVE_REPOL in case of ring trip<br>**Allowed operating modes:**<br>• DISABLED<br>• STANDBY<br>• ACTIVE_REVPOL<br>• GOUND_START |
| GROUND_START | Ground start is mainly used by PBXes.<br>Ground key detection is active.<br>No AC transmission.<br>Overtemperature and clock-fail detection is active.<br>Ring wire is feeding and tip wire is switched to high impedance. | **Allowed operating modes:**<br>• DISABLED<br>• GROUND_START_T2G if ground key is detected<br>• ACTIVE / ACTIVE_REVPOL<br>• RINGING / RINGING_REVPOL |
| GROUND_START_T2G | Ground key and hook detection is active.<br>No AC transmission.<br>Overtemperature and clock-fail detection is active.<br>Ring wire is feeding and tip wire is switched to ground. | **Automatic transition to:**<br>• ACTIVE if ground key is removed and off-hook is detected<br>**Allowed operating modes:**<br>• DISABLED<br>• GROUND_START<br>• ACTIVE / ACTIVE_REVPOL<br>• RINGING / RINGING_REVPOL |
| MESSAGE WAITING LAMP (ACTIVE_MWL) | Apply programmed MWL sequence to telephone line.<br>Hook detection is active.<br>Ground fault, overtemperature and clock-fail detection is active.<br>No AC transmission. | **Automatic transition to:**<br>• ACTIVE in case of off-hook<br>**Allowed operating modes:**<br>• DISABLED<br>• ACTIVE |
| ACTIVE_HOWL | Provide high AC gain to apply high level howler tone to the line.<br>On-hook detection possible.<br>Ground fault, overtemperature and clock-fail detection is possible.<br>Tone generation possible. | **Automatic transition to:**<br>• ACTIVE in case of on-hook<br>**Allowed operating modes:**<br>• DISABLED<br>• ACTIVE |
| ACTIVE_HOWL_REVPOL | Provide high AC gain to apply high level howler tone to the line.<br>On-hook detection possible.<br>Ground fault, overtemperature and clock-fail detection is possible.<br>Tone generation possible. | **Automatic transition to:**<br>• ACTIVE_REVPOL in case of on-hook<br>**Allowed operating modes:**<br>• DISABLED<br>• ACTIVE_REVPOL |
| CALIBRATE | Perform offset and gain calibration for DC feeding, transmit path and line monitoring circuit.<br>No line feeding and no hook detection. | **Automatic transition to:**<br>• DISABLED once calibration is finished<br>**Allowed operating modes:**<br>• DISABLED, but it will abort calibration |

**Table 3 Operating Mode Description** (cont'd)

| System State | Description | Transition |
|---|---|---|
| GR909 | Perform GR-909 line testing. | **Automatic transition to:**<br>• DISABLED once line testing is finished<br>**Allowed operating modes:**<br>• DISABLED, but it will abort line testing |
| CAP_MEAS | Perform capacitance measurement. | **Automatic transition to:**<br>• DISABLED once CAP_MEAS is finished<br>**Allowed operating modes:**<br>• DISABLED, but it will abort CAP_MEAS |

### 2.2.4.1 Emergency Shutdown

In addition to the operating modes that can be entered via commands, there is a system state which is entered automatically in the case of critical operating conditions, such as ground fault, high SLIC temperature or clock fail. This is the Emergency Shutdown (ESD) mode, as described in **Table 4**.

In the case of an overtemperature condition, the overtemperature end event is sent once the SLIC cools down to approximately 125°C. In the case of a ground fault condition, the ground fault end event is reported one ESD DUP Time period after the emergency shutdown mode was entered (see **Table 2**). In both cases, before programming any other operational mode, the DISABLED mode must first be set as indicated in **Table 4**. In order to simplify the application software, the DXS API automatically switches from ESD to DISABLED mode once it receives the event indicating the end of the fault condition on a given channel.

After that, it is recommended that the GR909 test is run to verify if the ground fault condition or any short circuit still persists. A short circuit may indeed be the root cause of the overtemperature event itself. As soon as the GR909 test does not show any resistive fault, the software may restore a specific operating mode, for example, the standard STANDBY voltage feeding on a given channel.

**Table 4 System State Description**

| System State | Description | Transition |
|---|---|---|
| ESD | Emergency Shutdown.<br>No voltage supplied to tip or ring.<br>No hook detection is possible.<br>DC/DC converter is enabled.<br>Overtemperature detection is active. | **Automatically entered:**<br>• Overtemperature detected<br>• Ground fault detected<br>• Clock fail detected<br>**Allowed operating modes:**<br>• DISABLED |

### 2.2.4.2 Clock Fail Handling

In the case of a clock fail, the chip reports the corresponding Internal Error event and both the channels are set to the ESD mode. In this case, the software has to reset the device. After a given amount of time, provided that the PCLK signal is available again, the DXS generates a “Boot finished event” at the end of the booting procedure. After this the host may configure the channels and set the desired operating modes again.

Nevertheless, in the case of scheduled clock fail events (for example, due to a remote CPE software update), it is also possible to disable the automatic switching to ESD mode via the DXS API **DxsClockFailLineFeedFreeze**. This action holds the DC feeding voltage during the software update phase, which may take several seconds to be completed, thus avoiding large feeding voltage drops. This may be very important in certain situations, for example where alarm systems are connected to the subscriber loop.

It is recommended to restore the default automatic switching to ESD mode after the software update phase has been completed (API: **DxsClockFailLineFeedUnFreeze**).

### 2.2.4.3 Sleep Condition

When both channels are in STANDBY or DISABLED mode and the mailboxes are empty, the DXS automatically switches to the sleep condition (lowest possible power consumption), if this feature has previously been enabled via the API function **DxsSleepEnable**. In this case, the DXS internal clock is switched off, and only the DC/DC converter is clocked. A wakeup out of the sleep condition is triggered when the subscriber goes off-hook, or if the DXS is accessed via a command on the SPI or CSI interface.

### 2.2.5 DC Feeding in ACTIVE Mode

The DC battery feed characteristic of the DXS consists of a constant current and a constant voltage region. The DC characteristic with normal and reverse polarity is shown in **Figure 6**.

In the constant current region, the DXS behaves like a nearly ideal current source with programmable value $I_{CONST}$[1)] (maximum 50 mA). However, if $V_{TR}$ exceeds a specific transition voltage, $V_{LIM}$ - $I_{CONST}$ x (2 x $R_{INT}$ + 2 x $R_{PROT}$), the SLIC's behavior changes to a voltage source with an internal impedance $R_{INT}$ of 20 Ω plus any external protection resistance $R_{PROT}$ for each tip and ring buffer. Therefore, in total the output impedance is 2 x $R_{INT}$ plus 2 x $R_{PROT}$. In this case the current flowing to the line will be lower than $I_{CONST}$. In the case of transients (for example, on-hook to off-hook transition) the SLIC limits the output current to typically 85 mA[2)]. The actual line voltage then depends on the DC line impedance $R_{LINE}$ ($V_{TR}$ = $R_{LINE}$ x $I_{CONST}$).

A low pass filter, implemented by means of an internal buffer and the external capacitor $C_{DC}$, ensures the stability of the DC feeding loop. The tolerances of the DC loop parameters are specified in chapter “DC and Ringing Characteristics” of the data sheets **[2]**, **[3]**, **[4]**.

In the constant current zone, the DC regulation loop is locked once the actual current reaches the programmed value. The DC loop regulation is started again if the error between the actual current and the programmed value is greater than 0.5 mA. Thus the output of the constant current zone is very flat, with a deviation from the average value of up to 0.5 mA.

XTCOS offers an "Automatic Sense Bias Enable" setting. If this is disabled, the current sensing range is 68 mA. If this feature is enabled, then the bias current for the current sensor is reduced to the actual required sensor range. This means that, for example, during on-hook the sensor range will be reduced to typically 23 mA. Therefore the on-hook current from the battery supply can be reduced by approximately 30%.

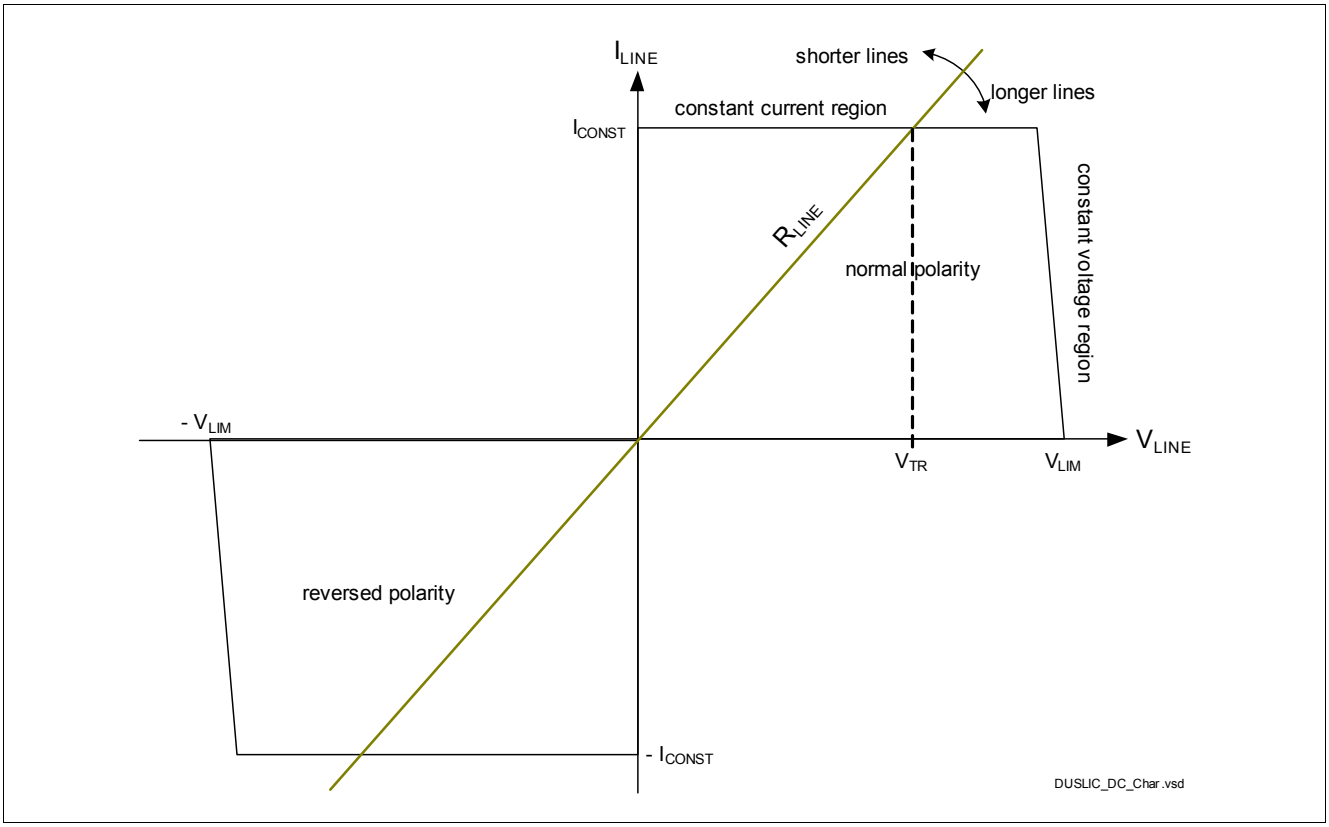


**Figure 6 DC Characteristic of the DXS**

1) In the constant current region of DC feeding, the current is $I_{CONST}$ + algorithmic error (< ±0.5 mA) + analog gain error (< 5%).

2) Output current limitation of SLIC specified in chapter “DC and Ringing Characteristics” of the data sheets **[2]**, **[3]**, **[4]**.

### 2.2.6 AC Transmission Characteristics

In the receive direction, the DXS converts voice data (via the PCM interface) from the network and applies it to the subscriber line. In the transmit direction, the transversal current on the line is sensed and fed to the Analog Front End. The transversal (sometimes called metallic) sensed current on the line includes both the receive and transmit components. The DXS separates the received components from the transmitted components via a digital transhybrid circuit.

The signal flow for one voice channel within the DXS is shown in **Figure 7**.

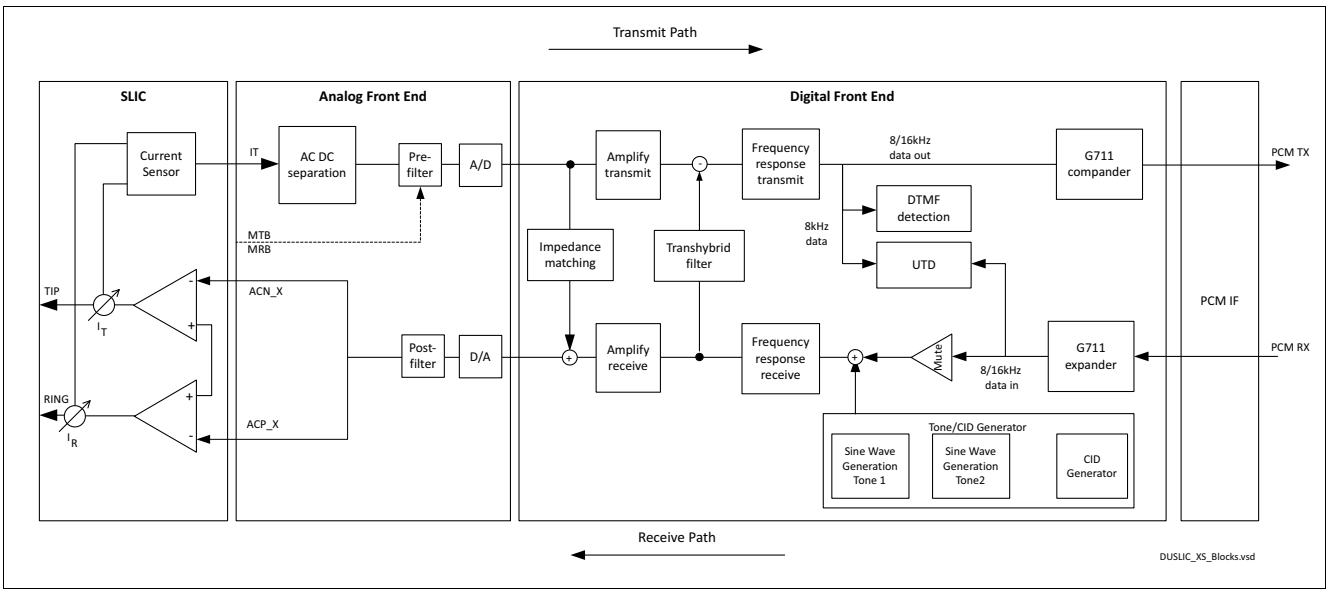


**Figure 7 Analog Line Module for DXS, Signal Flow for an Analog Channel**

#### 2.2.6.1 Transmit Path

The current sense signal (IT) is converted to a voltage by an internal transimpedance converter. The DC portion of the IT is removed. After this, the voltage is filtered by an anti-aliasing low pass filter (pre-filter). The A/D conversion is performed by a 1-bit sigma-delta converter. The digital signal is further down-sampled and routed through programmable gain and filter stages. The coefficients for the filter and gain stages are programmed to meet country or customer specific requirements. The digital signal is transferred to the controller for further processing (for example, G.711 A-Law or µ-Law).

#### 2.2.6.2 Receive Path

Digital voice data is transferred via the PCM Interface to the controller, which performs low pass filtering, frequency response and gain correction. The digital data is then passed on to the Analog Line Module (ALM - see also **Figure 3**) for further up-sampling and digital-to-analog conversion. After smoothing by post-filters in the DXS, the AC signal is fed to the SLIC, where it is superimposed on the DC signal.

### 2.2.6.3 Impedance Matching and Hybrid

The DXS feeds the voice signal to the line (receive direction) and senses the voice signal coming from the subscriber (transmit direction). The AC impedance of the DXS and the load impedance need to be matched to maximize power transfer as well as two-wire return loss. The two-wire return loss is a measure of the impedance matching between a reference line impedance, representing the average of the transmission lines, and the AC termination of the DXS.

Impedance matching is carried out digitally within the DXS by integrated impedance matching feedback loops. The loops feed the transmit signal back to the receive signal path, thereby synthesizing the programmed impedance, which also includes the external resistors ($2*R_{PROT}$ ) between the protection circuit and the DXS (see chapter “Application Circuit” of the data sheets **[2]**, **[3]**, **[4]**). The device can be adapted to requirements anywhere in the world with conventional linecard designs without requiring any hardware changes. Possible values for the line impedance can be seen in **Figure 8**.

The filter coefficients for impedance matching are calculated using the DXS coefficient calculation tool XTCOS.

The Transhybrid Balance is a measure of the local echo cancellation. The voice signal from the PCM interface of the DXS is first D/A converted in the RX path and then amplified differentially by the SLIC. Therefore it is superimposed on the signals coming from the subscriber loop, which share the same bandwidth. The two components are separated in the digital TX path using a programmable filter bank to guarantee the specified four-wire return loss.

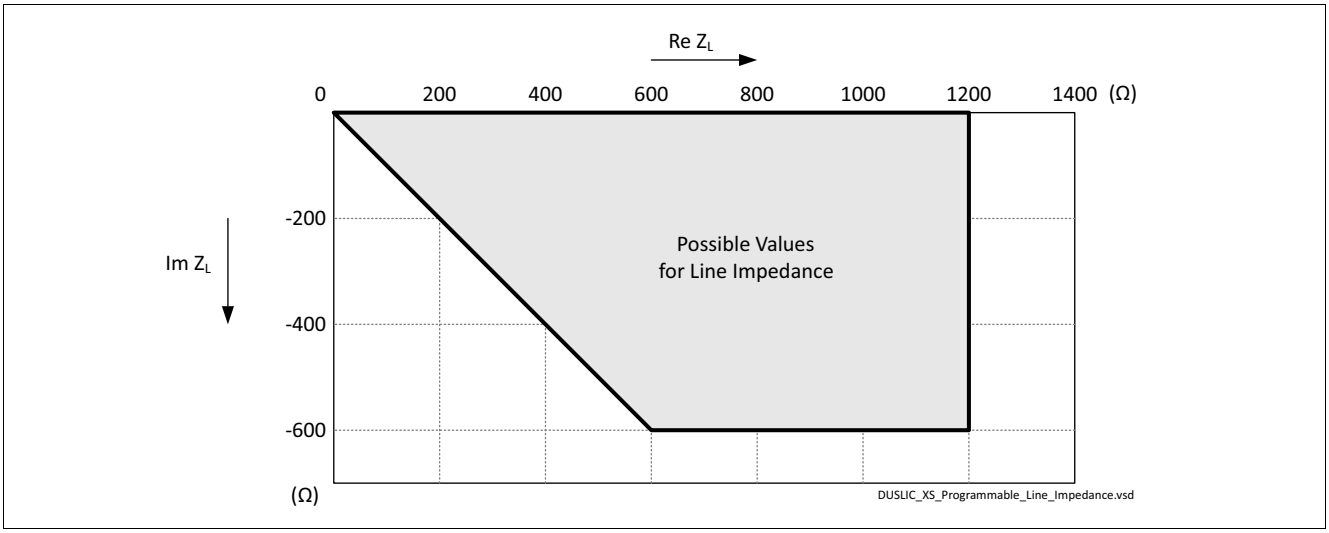


**Figure 8 Programmable AC Impedance**

### 2.2.6.4 Metering (TTX) Signal Generation

Teletax (TTX) metering is used to provide billing information for dedicated telephone lines. The TTX signal is generated by the DXS codec and amplified by the SLIC.

The DXS supports teletax metering for 12 kHz and 16 kHz signals up to 1 $V_{RMS}$ over the specified TTX Termination Impedance, see **Table 2**. However, the maximum amplitude of 1 $V_{RMS}$ cannot be reached with any combination of AC Impedance and TTX Termination Impedance.

For example, it is not possible to achieve 1 $V_{RMS}$ across a load of 200 Ω and with a DXS AC Impedance of 900 Ω, because the output impedance of the TTX generator becomes too large compared to the load and the TTX generator cannot indefinitely increase its output voltage. As a general rule, in order to get the maximum 1 $V_{RMS}$ TTX amplitude, the AC and TTX Impedances should be approximately the same value at the selected TTX frequency. If the programmed amplitude cannot be achieved, the XTCOS generates a warning and it is necessary to either reduce the programmed TTX amplitude or accept the automatic limitation of the BBD calculation core, documented in the BBD Result file (*.RES).

All TTX parameters can be configured using the corresponding XTCOS fields, see **Figure 9**. The slope time, i.e the duration of the transient to reach the desired amplitude, and the burst length can also be configured.

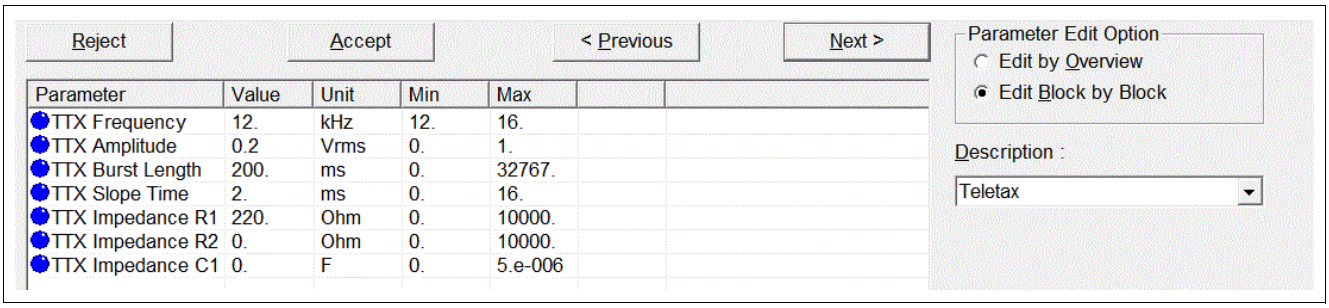


**Figure 9 Screenshot of XTCOS TTX Parameters**

## 2.2.7 Ringing

Due to the technology used for the SLIC, a balanced sinusoidal ringing voltage of up to 144 V (DC + AC Amplitude in total) can be generated on-chip, without a need for an external ringing generator. The battery voltages for the ring signal are generated by the DC/DC converter, which is controlled by the integrated pulse width modulator. The system supports up to 5 REN (see **Chapter 2.2.7.1** for the definition). The ringing frequency is programmable from 15 Hz to 50 Hz with a resolution finer than 0.2 Hz.

The DXS provides quasi-balanced or unbalanced ringing. In the case of unbalanced ringing, the maximum ring amplitude is reduced. Quasi-balanced ringing provides the advantage that, with the same peak $V_N$ voltage, the ring amplitude is higher. In addition, the $V_N$ supply can follow the envelope of the ringing signal, thus further reducing power consumption (see **Quasi-balanced Ringing** in **Chapter 2.2.7.3**).

### 2.2.7.1 Ringer Load

A typical ringer load can be thought of as a resistor in series with a capacitor. Ringer loads are usually described as a Ringer Equivalence Number (REN) value. REN is used to describe the on-hook impedance of the terminal equipment and is actually a dimensionless ratio that reflects a specific load. REN definitions vary from country to country. A commonly used REN is described in FCC Part 68, which defines a single REN as either 5 kΩ, 7 kΩ or 8 kΩ of AC impedance at 20 Hz. The impedance of an n-multiple REN is equivalent to parallel connection of n single RENs. In this manual, all references to REN assume the 7 kΩ model.

Examples for 1 and 5 REN loads, typically used in the US, are given in **Figure 10**:

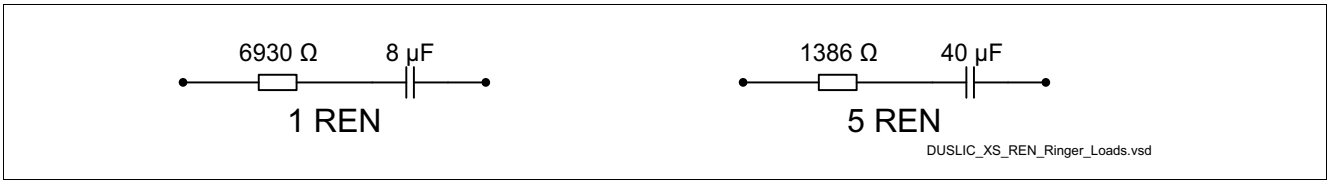


**Figure 10 Typical Ringer Loads of 1 and 5 REN According to FCC Part 68**

### 2.2.7.2 Ring Trip Detection

Ring Trip Detection (RTD) is implemented by three different methods: DC RTD, AC RTD and Fast RTD. The AC and Fast RTD methods are suitable for short lines (< 1 kΩ loop resistance) and for low power applications, since a DC voltage can be avoided to reduce the battery voltage feeding for a given ringing amplitude.

DC RTD is recommended for long lines. It provides a more reliable detection of ring trip by sensing the DC portion of the ring current.[1)]

#### 2.2.7.2.1 DC Ring Trip Detection (DC RTD)

This is the most reliable RTD method. A DC offset is generated together with the ringing signal; therefore a transversal DC current starts to flow when the subscriber goes off-hook. The current is sensed by the DXS, which integrates the sensed line current $I_{TRANS}$ over one ringer period to filter out the AC components. The result of the integration therefore represents the DC current, which is zero when a pure ringer load is connected.

If the DC current exceeds the programmable DC Ring Trip threshold, off-hook is indicated. The tip-ring voltage for the DC RTD (ringing offset) is programmed via coefficients and is generated by the DXS chip in ringing mode. This ring offset is automatically switched on during RINGING mode.

The Fast Ring Trip threshold is monitored in parallel to the DC Ring Trip threshold. If the ringing current exceeds the Fast Ring Trip threshold for at least 5 ms during one ring period then, at the end of the ring period, the ringing is switched off, the chip is set to ACTIVE and off-hook is reported.

#### 2.2.7.2.2 AC Ring Trip Detection (AC RTD)

An off-hook event in ringing mode can be recognized by means of the AC RTD method. This is executed by rectifying the ring current $I_{TRANS}$, integrating it over one ringer period and comparing it to a programmable AC Ring Trip threshold. If the integrated ringing current exceeds the programmed threshold, the ringing signal is switched off at the next ring voltage zero crossing point and the chip is automatically set to ACTIVE mode.

#### 2.2.7.2.3 Fast Ring Trip Detection (Fast RTD)

In the case of Fast RTD the ringing signal is switched off immediately, as soon as ring trip is detected. Compared to DC RTD this has the advantage that the high current on the line and, therefore, the high current from the supply voltage is switched off faster and not only at the next ring voltage zero crossing point. The ringing current is simply rectified and compared to the programmable Fast Ring Trip threshold. If the current exceeds the threshold for at least 5 ms, the ringing is switched off, the chip is set to ACTIVE and off-hook is reported.

DC RTD continues to operate in parallel to Fast RTD. If the Fast Ring Trip current threshold does not trigger, for example, in the case of long loops, then DC RTD is still in operation. Therefore, the thresholds for both RTD methods (Fast RTD and DC RTD) are monitored. The only difference is that for DC RTD the switch-off will always occur at the ring voltage zero crossing point, while for Fast RTD the switch-off occurs immediately.

1) With rectangular ringing waveforms (crest factor = 1), DC Ring Trip cannot be detected. In this case the use of AC or Fast Ring Trip is recommended.

### 2.2.7.3 Ringing Methods

Application requirements differ with regard to ringing amplitudes, power requirements, loop length and loads. The DXS options include two different ringing methods for these applications - the quasi-balanced and unbalanced ringing methods.

The phone itself cannot distinguish between balanced and unbalanced ringing. For a comparison between balanced and unbalanced ringing, see also ANSI T1.401- 2000 document **[15]**.

The sinusoidal ringing signal is generated in the Digital Front End of the DXS, thus allowing fully programmable ringing amplitude and frequency. The generated ring signal is propagated through the DC path and is differentially generated after the D/A conversion at the internal SLIC interface.

#### Quasi-balanced Ringing

Significant ring power reduction is achieved by this approved ring concept. The main idea is to extend the well-known concept of “minimum battery voltage generation” from static DC feed to (slowly) varying ring signals. However, to make this approach highly efficient, the DXS utilizes a patented signal shape called “quasi-balanced”, which is neither balanced nor unbalanced.

With conventional balanced ringing as depicted in **Figure 11** (a), the signals on tip and ring are differential low frequency sine waves (neglecting DC components) and the circuit is supplied by a constant voltage $V_N$ somewhat larger than their peak-to-peak value. The common mode potential at the line interface $V_{CML}$, i.e. the mean value of $V_{TIP}$ and $V_{RING}$, is constant and equal to half the supply voltage:

$$V_{CML} = \frac{V_{TIP} + V_{RING}}{2} = \frac{V_N}{2} \quad (1)$$

The difference between $V_N$ and the line voltage $V_{TR}$ = $V_{TIP}$ - $V_{RING}$ is dropped on-chip and unavoidably leads to high power dissipation. An improvement is clear: if $V_N$ could track the negative signal envelope, power dissipation would be reduced. However, the power saving potential is limited, as a symmetrical tracking approach on the positive side cannot be realized easily.

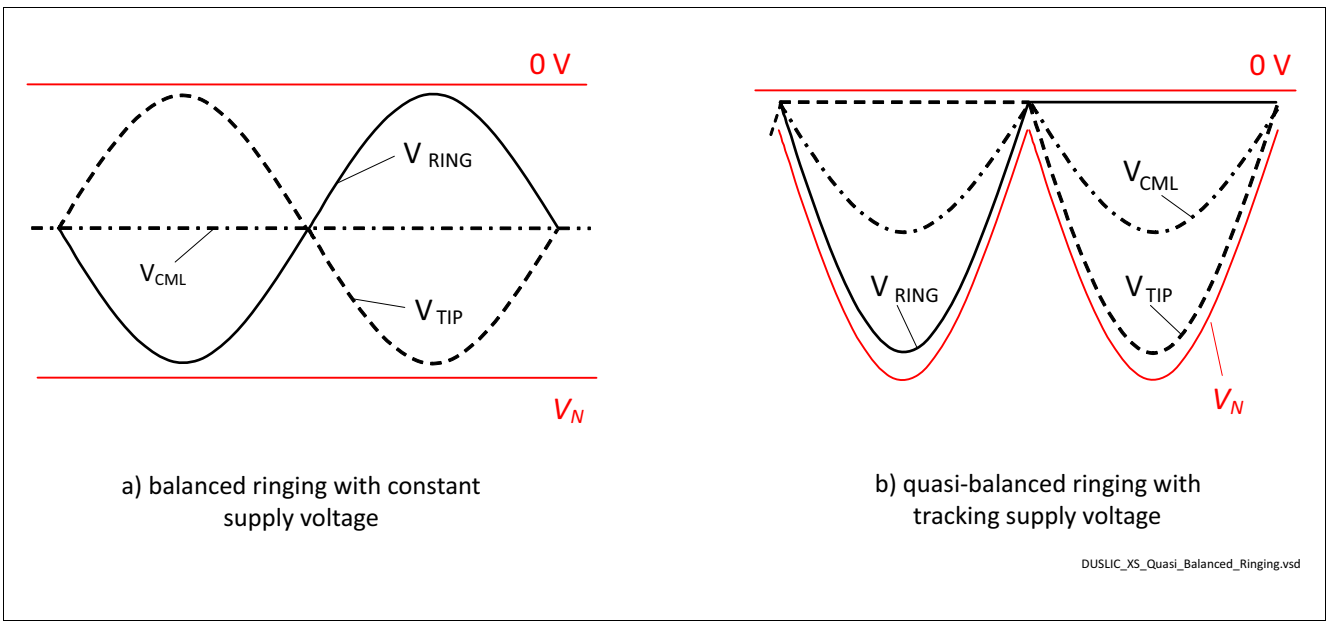


**Figure 11 Comparison of Ringing Waveforms**

The situation changes to the “quasi-balanced” signal shape of **Figure 11**. Here both line voltages $V_{TIP}$ and $V_{RING}$ alternately exhibit negative sine half waves for half a ring period, staying close to zero for the other half of the period. It is important that, compared to the normal balanced waveform, the differential voltage on the line, $V_{TR}$, remains an unchanged large sine wave. However, the positive envelope is now constant. Consequently, $V_{CML}$ is not constant any more, but also shows the sine half wave shape. As is evident from **Figure 11**, if now the supply voltage $V_N$ is generated to track the negative envelope, the voltage drop in the SLIC, $V_N$ - $V_{TR}$, is minimized at any time to a constant few volts, thus minimizing the resulting on-chip power dissipation. **Equation (1)** is still valid, i.e. the common mode potential equals half the supply voltage.

The voltage $V_N$ is generated by rectifying the output signal from the ring signal generator and adding a constant overhead voltage (see **Figure 12**).The voltage overhead of the DXS is programmable and should be set to a value that is at least as big as the required voltage drop of the SLIC buffer for the ringing current (refer to the figure showing “Typical Voltage Drop on Tip and Ring Buffers in ACTIVE and RING_BURST Operating Modes” in **[2]**, **[3]**, **[4]**). The required common mode voltage ($V_{CML}$) is then just half of $V_N$ (according to **Equation (1)**). Both signals can be applied to the line by use of dedicated reference voltage blocks and corresponding DACs.

It is worth mentioning that the chosen architecture does not require any additional circuitry compared with the traditional approach. However, the external DC/DC converter components have to be dimensioned to support ring voltage tracking. In particular, this means the use of a relatively low converter capacitance. The new ringing method is very effective in power critical applications, typically halving the power dissipation during ring burst.

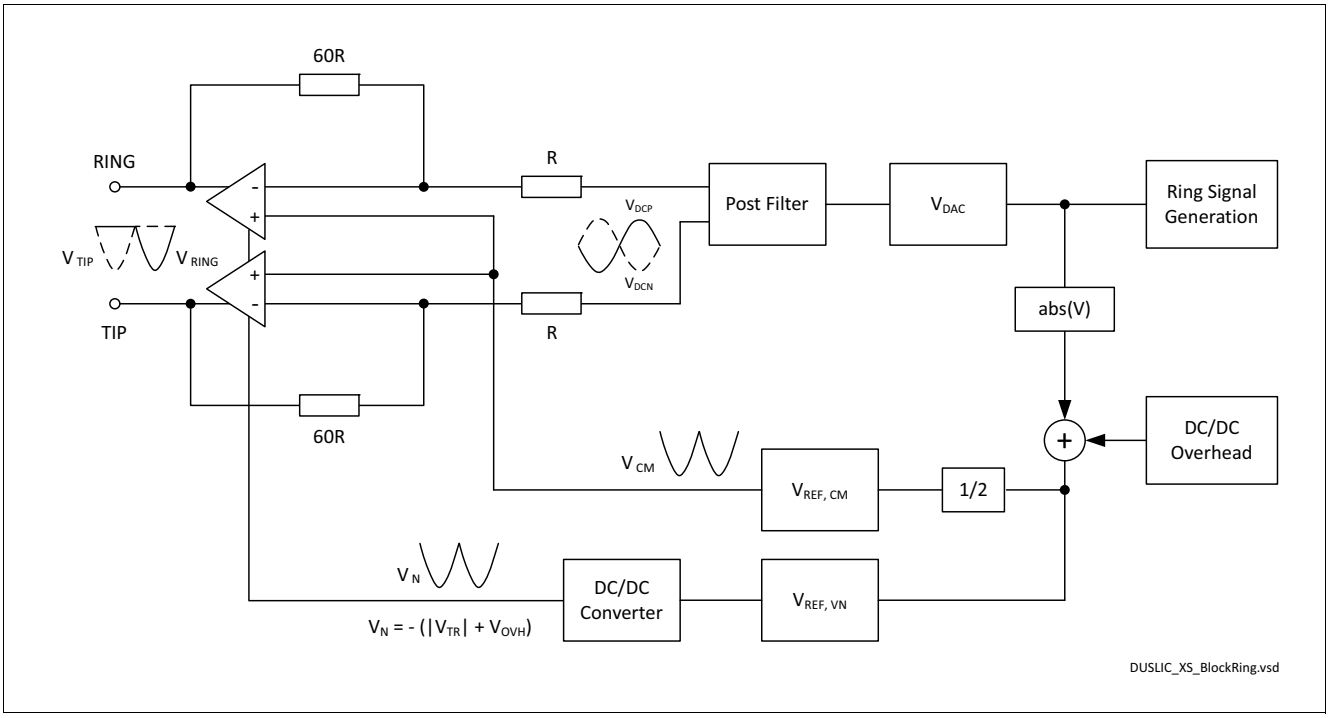


**Figure 12 Details of DC Path with Generation of Quasi-Balanced Ring Signal**

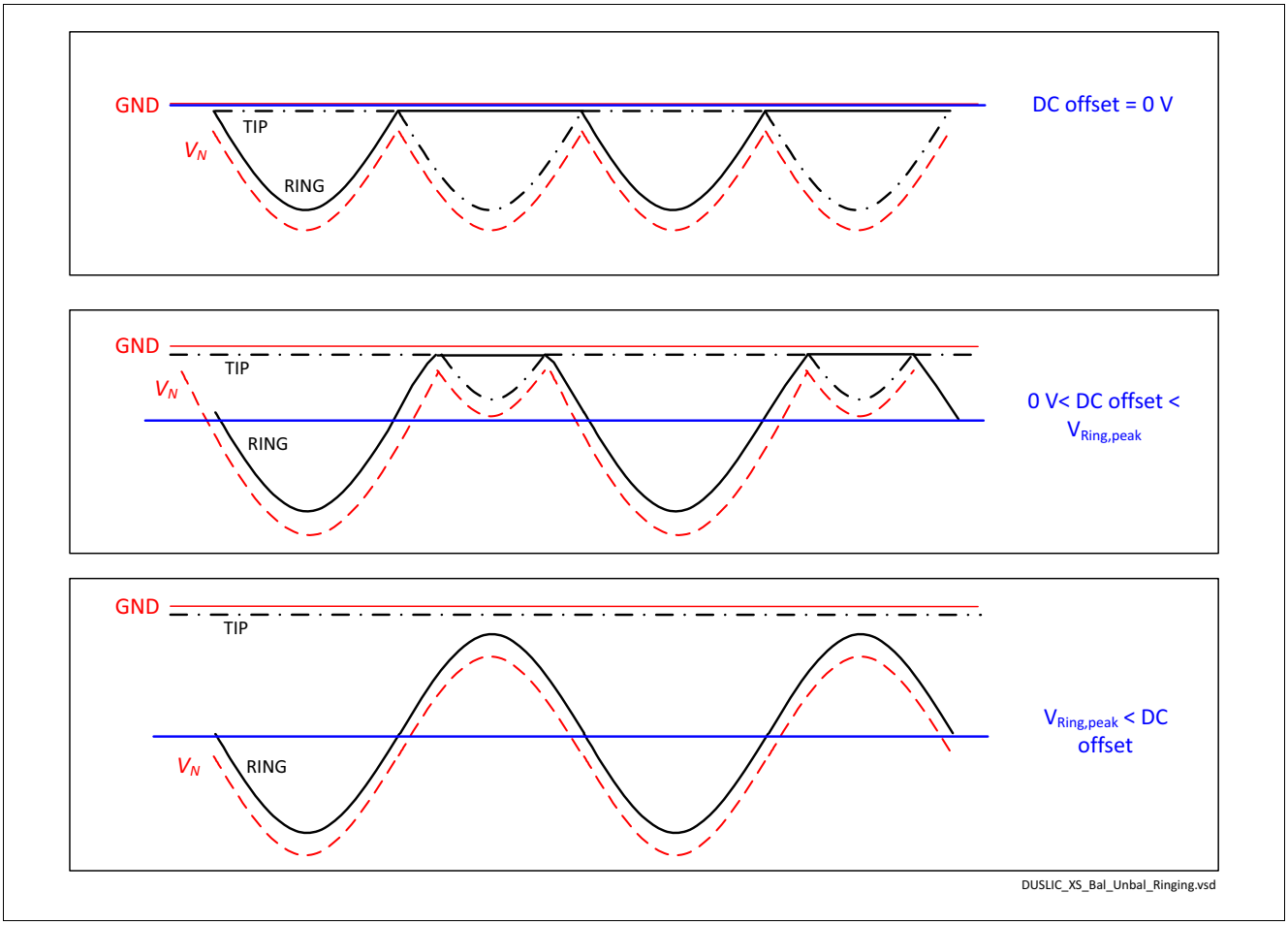


**Figure 13 Quasi-balanced and Unbalanced Ringing Dependent on DC Offset**

### Unbalanced Ringing

**Figure 13** shows that it is easy to generate unbalanced ringing using the DXS. If the ringing DC offset is set equal to or higher than the peak ringing amplitude $V_{Ring,peak}$, then unbalanced ringing is generated automatically. Note that the maximum differential output voltage is 144 V. Therefore, the DC/DC converter external components have to be chosen to withstand a $V_N$ of 150 V.

The maximum unbalanced ringing voltage will therefore be limited to 50 $V_{RMS}$. In this case, the ringing DC offset should be set to 72 V. All the values can be configured via XTCOS.

### Quasi-balanced Ringing with Constant $V_N$

**Figure 13** shows the standard DXS ringing signals, depending on different DC offsets. By default, $V_N$ tracks the $V_{TIP}$ and $V_{RING}$ ringing voltages in order to minimize the average power consumption. However it is still possible to disable this feature and supply the channel in ringing mode with a constant $V_N$ voltage, whose value is automatically calculated by the firmware and is dependent on the programmed ringing amplitude, offset and overhead voltages, see **Figure 14**.

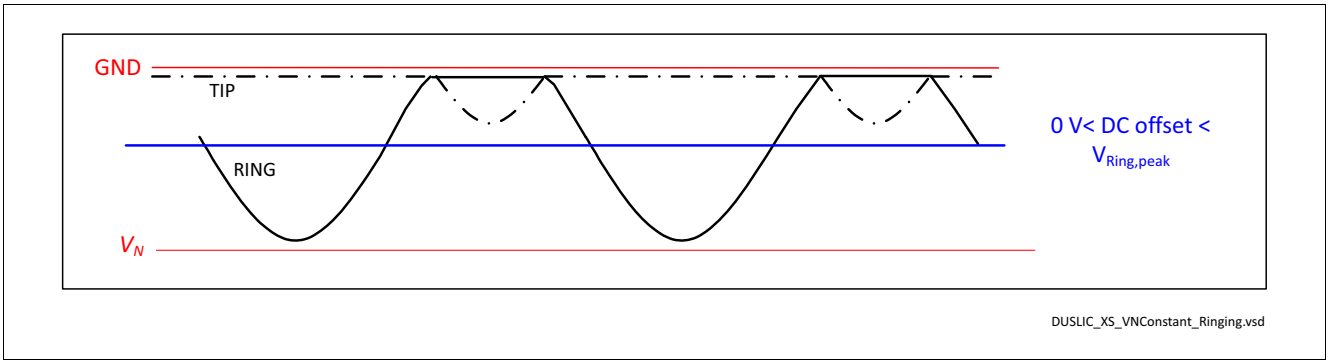


**Figure 14 Ringing Waveforms with Constant $V_N$**

Supplying a constant $V_N$ generally increases the average power consumption during ringing bursts but reduces the peak power consumption: the external capacitor connected to $V_N$ is charged only once, which allows the maximum current supplied during the ringing phases to be reduced.

In order to program this feature, it is sufficient to set the XTCOS flag "VN voltage during Ringing" to “Constant” (default is “Tracking”), see **Figure 15**. The flag is available in the "Low Power Features" menu.

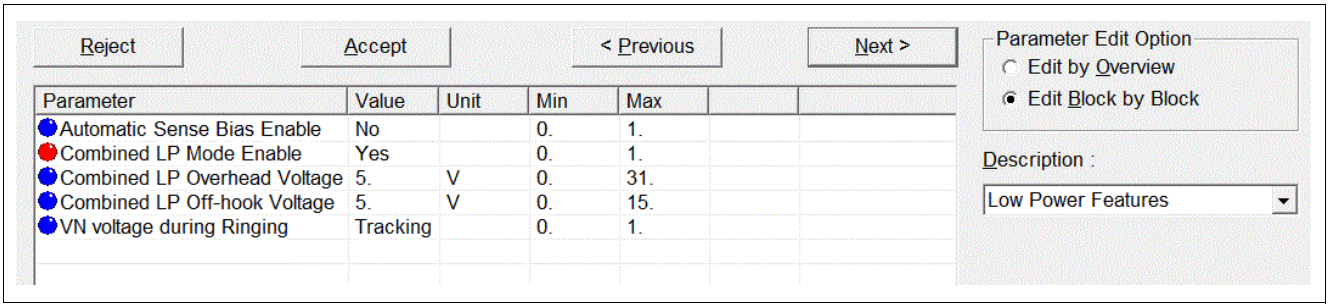


**Figure 15 Screenshot of XTCOS Low Power Features**

### 2.2.8 Ringing Current Regulation

With the DXS, it is possible to reduce power consumption on shorter lines by means of automatic load-dependent adjustment of the ringing voltage. This internal ring current regulation is patented by Intel.

In order to define the ringing requirements, the following relevant parameters need to be identified:

- The maximum subscriber line length that needs to be supported.
- The number of telephones that will need to be connected in parallel.
- The minimum ringing voltage required at the end of the longest line when the maximum number of telephones are connected.

The maximum line length defines the maximum loop resistance that needs to be compensated for. Even if the supported line length is very small (e.g. <100 m), there may be a defined loop resistance that needs to be considered. The maximum number of telephones connected in parallel to the line is usually provided in REN (Ringer Equivalent Number, see **Chapter 2.2.7.1**). Typically, a system needs to support up to 5 REN.

The above three parameters are usually used to calculate the open-loop voltage at the FXS port ($V_{Ring}$). The subscriber loop as seen at the FXS port of the DXS is modeled in **Figure 16**.

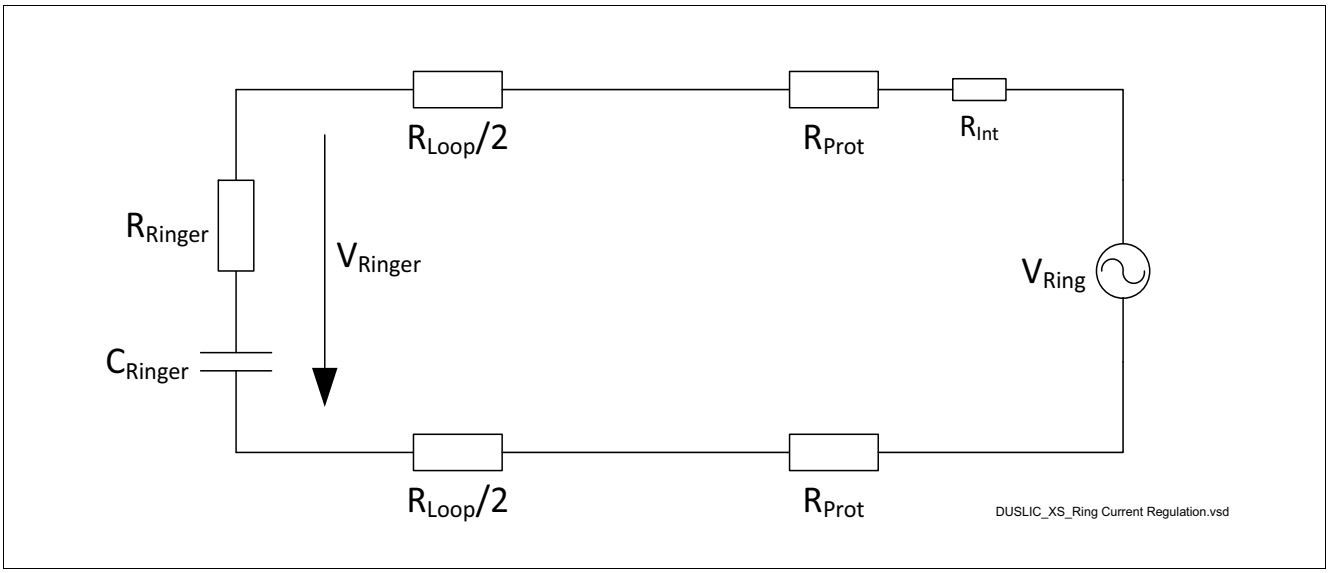


**Figure 16 Subscriber Loop Model for Ring Current Regulation**

The voltage drop across the loop resistance has to be compensated for by a higher output voltage $V_{Ring}$ at the DXS. The maximum required output voltage ($V_{Ring,max}$) is defined as that required to ring the maximum number of telephones connected at the end of the longest line. The current flowing in this case is the maximum current that is required to ring the maximum number of telephones ($I_{Ring,max}$). It will not be possible to connect more telephones in parallel, so that the current in the longest loop will always be less than $I_{Ring,max}$.

However, the line current is higher than $I_{Ring,max}$ when the maximum number of telephones are connected to a short loop. In this case, automatic ring current regulation reduces $V_{Ring}$ to provide a line current of exactly $I_{Ring,max}$, as this current is sufficiently large to ring the maximum number of telephones. By limiting the ringing current, power consumption can be reduced without violating the specification and the functionality of the telephone system.

Both the $V_{Ring,max}$ and $I_{Ring,max}$ values are provided as configuration parameters using XTCOS (see **Table 2**). The parameter **Ringing Amplitude** is used to determine the value of $V_{Ring,max}$, and the **Maximum Ring Current (for ring current regulation)** is used to determine $I_{Ring,max}$. In addition, the **Minimum Ring Voltage (for ring current regulation)** XTCOS parameter can be configured to ensure that the ring current regulation does not output a voltage below a certain value ($V_{Ring,min}$).

Operation of automatic ring current regulation within the parameters $V_{Ring,max}$, $I_{Ring,max}$, and $V_{Ring,min}$ is illustrated in **Figure 17**. In the figure, $Z_{TOTAL}$ is defined as $Z_{Ringer}$ + $R_{Loop}$ + $R_{Int}$ + 2 * $R_{Prot}$ (see also **Figure 16**).

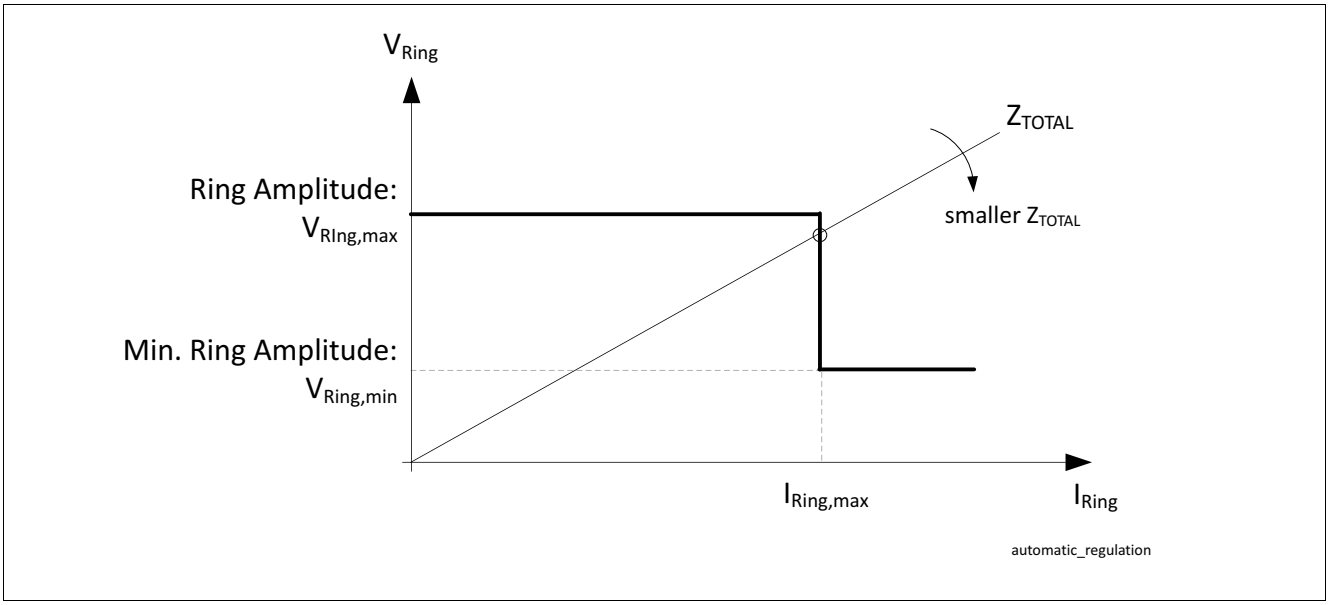


**Figure 17 Ring Current Regulation Parameters**

The ring regulation starts with $V_{Ring,max}$ for the first ring burst after reset. The programmed ringing voltage ($V_{Ring}$) is provided at the source of the line (DXS FXS port). If the measured current is above $I_{Ring,max}$, the ringing voltage $V_{Ring}$ is reduced. As time progresses, the ring regulation stores the last operating point and starts the next ringing bursts from this point.

**Example:**

According to GR-57, a DLC system must provide a minimum ringing voltage of 40 $V_{RMS}$ across a ringing load of 5 REN at the end of any line with a loop resistance $R$, where $R$ is the smaller value between ($R_{DC}$ - 400) and 930 Ω.

A ringing load of 5 REN implies a ringer impedance of 1400 Ω at 20 Hz. This results in a maximum required line current of 28.56 mA.

Example: Take $R$ = 700 Ω. The required ringing voltage $V_{Ring}$ is calculated as follows:

$V_{Ring}$ = 40 $V_{RMS}$ * (1400 Ω + 112 Ω + 700 Ω) / 1400 Ω = 63.2 $V_{RMS}$

The value 112 Ω is obtained by taking the 40 Ω internal resistance plus the 2 * $R_{Prot}$ resistance into consideration. From the above calculation, a $V_{Ring}$ value of 65 $V_{RMS}$ can be chosen. The $I_{Ring,max}$ value can, for example, be set to 30 mA. The $V_{Ring,min}$ value can be set to 45 $V_{RMS}$ to achieve a minimum voltage.

These settings allow the requirements of GR-57 to be fulfilled. In the case of maximum line length, the minimum required voltage will be available at the subscriber end for 5 REN. There will be a significant improvement when ring current regulation is used for short lines.

Without ring current regulation, the power consumption on the line can be calculated as follows:

$P_{Standard} = 65^2 / (1400 + 112) = 2.8$ W

Using ring current regulation, the voltage can be reduced to significantly reduce the power consumption:

$P_{RingCurrentRegulation} = 45^2 / (1400 + 112) = 1.34$ W

### 2.2.9 Hook Detection in ACTIVE Mode

In ACTIVE mode, the off-hook detection includes sensing the transversal line current on the ring and tip wires and comparing it with a programmable threshold. The transversal current is defined as: $I_{TRANS} = (I_R + I_T)/2$, where $I_R$, $I_T$ are the loop currents on the ring and tip wires.

$I_{TRANS}$ is converted to a voltage by a transimpedance amplifier. This voltage is compared with a programmable threshold, which also includes a hysteresis in ACTIVE mode.The off-hook information is filtered by a persistence counter in order to suppress line disturbances.

### 2.2.10 Hook Detection in STANDBY Mode

In STANDBY mode, the off-hook detection is performed by limiting the maximum output power of the DC/DC converter. During the on-hook condition, the DC/DC converter is able to generate the required output voltage. When the subscriber goes off-hook, the DC/DC converter cannot generate the desired output voltage because the output power of the DC/DC converter is limited. This is detected and the DXS switches to ACTIVE mode automatically.

By default, the maximum output power of the DC/DC converter is set to 400 mW. When considering the recommended inverting buck-boost DC/DC converter circuit (see chapter "Application Circuit" of data sheets **[2]**, **[3]**, **[4]**), for a 40 V STANDBY output voltage, the off-hook current threshold is approximately 10 mA.

For other configurations or modified DC/DC external components, the DC/DC configuration can be changed in XTCOS.

### 2.2.11 Ground Start Signaling

In contrast to a loop start system where the seizing of the line is done by loop closure, the seizing of a line is performed via a reference to ground in a ground start system. Ground start is mainly used for PBXes.

**Figure 18** shows the corresponding state machine implemented in the DXS. The handling of the line is similar to the loop start configuration. In the on-hook condition, the line is set to GROUND_START mode using the API function **DxsLineModeSet**. In this mode the tip wire is high impedance while the ring wire applies the same voltage as it would in ACTIVE mode.

Current regulation still operates during the complete ground start sequence. As long as there is only current in the ring wire, the transversal current is only half the value of the current in the ring wire. The current in the ring wire is regulated to a fixed value matching the ground key detection threshold of the ground key comparator (corresponding to 15 mA).

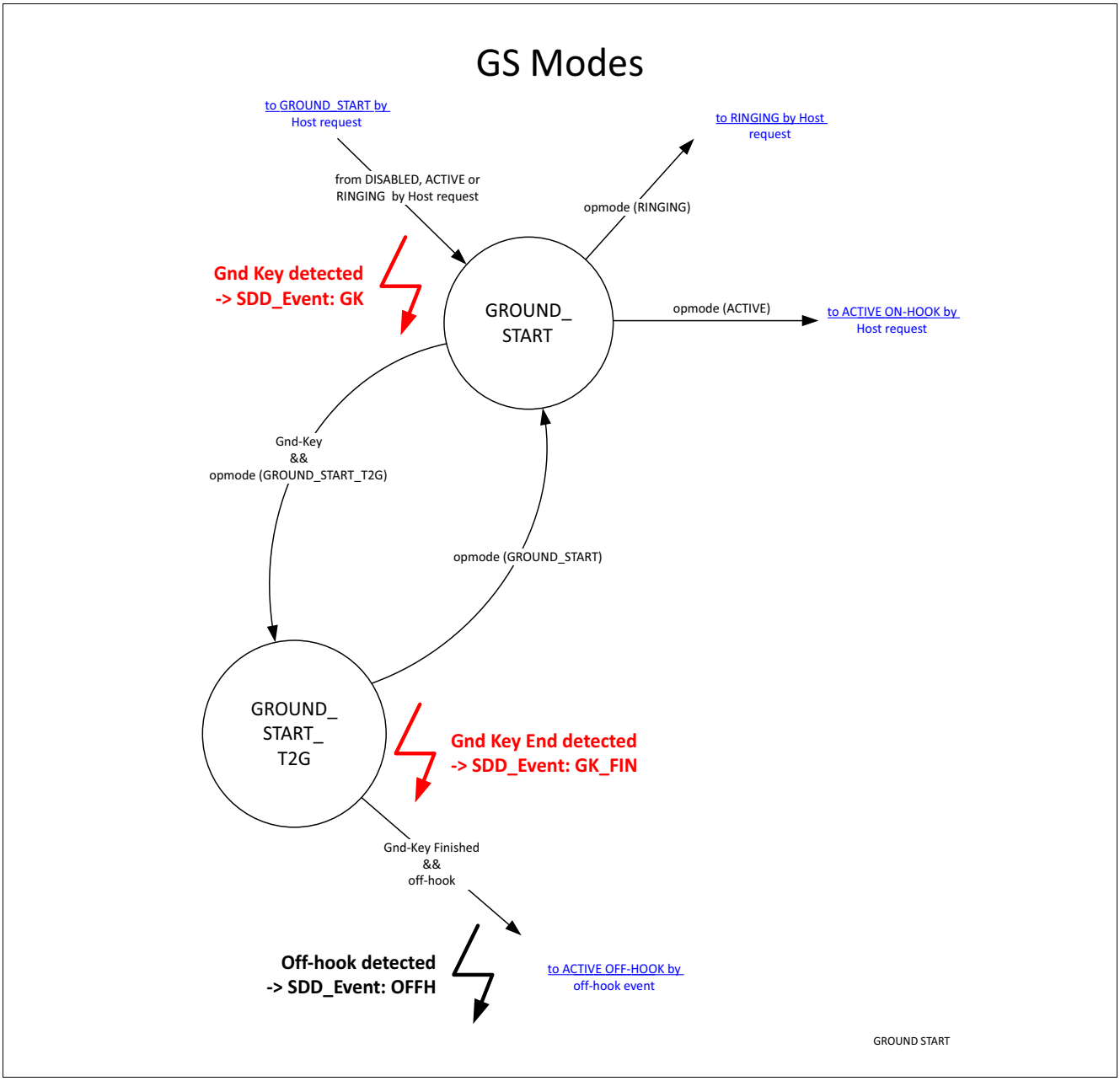


**Figure 18 Ground Start State Machine**

In the case of an outgoing call, the terminal (PBX) connects the ring wire to ground. This is recognized by the DXS and, after a configurable debounce time, this signaling is reported via a ground key event.

If the switch has no free transmission path available, the state machine stops and waits until the ring wire is released again by the terminal (the DXS reports a ground key end event).

If there is a transmission path available, the application has to configure the line to GROUND_START_T2G mode using the API function **DxsLineModeSet**. This means that the DXS connects the tip wire to ground. This indicates to the terminal that there is a transmission path available. The terminal then releases the ground connection and closes the loop.

This is detected by the DXS and the state machine reports a ground key end event followed by an off-hook event. The DXS changes to ACTIVE mode automatically. If the terminal does not close the loop, the state machine stays in GROUND_START_T2G mode until the application configures the line to GROUND_START mode again.

### 2.2.12 Ground Key / Ground Fault Detection

A ground fault or a ground key is detected via two independent longitudinal current thresholds. The threshold for the ground key detection is ±9.4 mA and for the ground fault detection is ±27.6 mA.

The ground key threshold is filtered via a programmable debounce (DUP) time (see XTCOS). Therefore, if the longitudinal current exceeds the ground key threshold for longer than this debounce time, then a ground key event is reported. This algorithm allows a type of sine wave suppression as it is expected that most of the longitudinal currents will come from AC coupling.

The ground fault indication is filtered via the programmable emergency shutdown debounce (DUP) time (see XTCOS). Therefore, if the longitudinal current exceeds the ground fault threshold for longer than this debounce time, a ground fault event is reported. The DXS automatically changes to the emergency shutdown mode where the tip and ring buffers are switched off to prevent damage to the device.

A ground fault end event is reported once the corresponding ground fault debounce time has expired after the switch to emergency shutdown mode. To exit from emergency shutdown mode, the channel must be set to DISABLED using the API function **DxsLineModeSet**.

### 2.2.13 Message Waiting Indication with Glow Lamp (MWL)

Message Waiting Indication with Glow Lamp (MWL) can be performed using a glow lamp at the subscriber phone[1]. Current does not flow through the lamp until the voltage reaches a threshold value above approximately 80 V. The neon gas in the lamp starts to glow at this threshold. When the voltage is reduced, the current falls under a certain threshold and the lamp glow is extinguished.

The hardware circuitry is shown in **Figure 19**. The figure shows a typical telephone circuit with the hook switch in the on-hook mode, together with the impedances for the on-hook (ZR) and off-hook (ZL) modes.The glow lamp circuit also requires a resistor ($R_{MW}$) and a lamp (MW Lamp) built into the phone. When activated, the lamp must be able to either blink or remain on constantly.

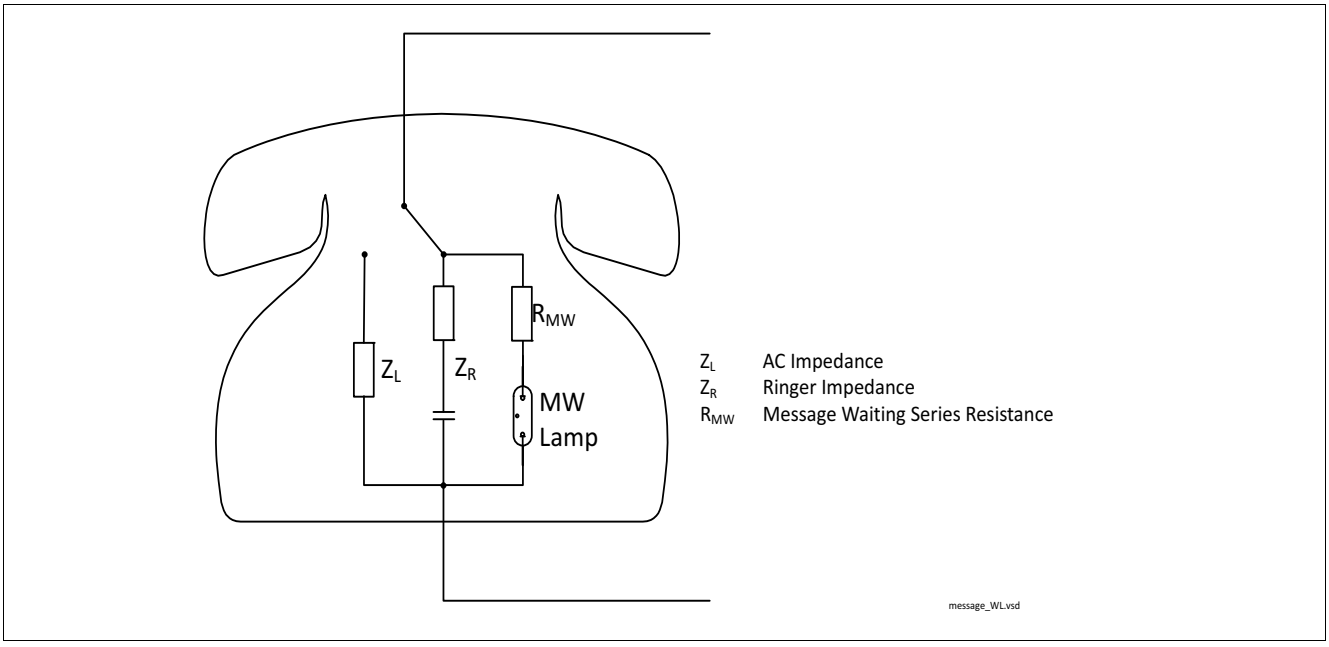


**Figure 19 MWL Circuit with Glow Lamp**

1) The DXS system also supports MWI using FSK (for more details see **[6]**). To distinguish between the two methods, the abbreviations MWL (with glow lamp) and MWI (with FSK) are used.

The MWL sequence on tip and ring is shown in **Figure 20**. The currents during the ramp are caused by loading the ringer capacitor. The current when the lamp is on depends on the lamp characteristics. The off-hook level during the MWL ramp has to be chosen such that high current during the ramp does not generate an off-hook.

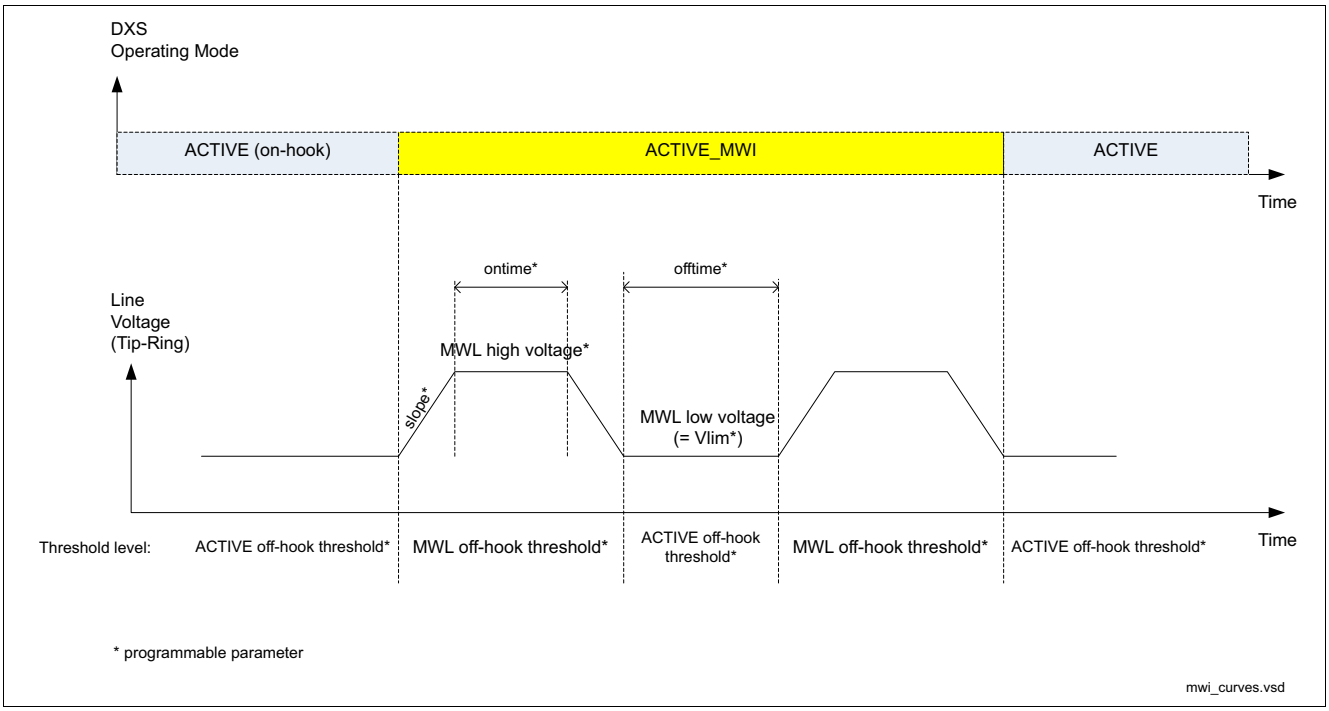


**Figure 20 MWL Line Voltage and Current**

### MWL Cadence

Automatic cadence is supported by a programmable ontime and offtime as shown in **Figure 20**. When offtime is set to zero, the output voltage stays high until the operating mode is changed back to ACTIVE. The parameters for the message waiting lamp are calculated using XTCOS and set in the BBD file.

### Switch on the MWL

The message waiting lamp is activated by setting the line to ACTIVE_MWI mode using the API function **DxsLineModeSet**. The line voltage starts ramping up from the line voltage of ACTIVE mode ($V_{lim}$) until it reaches the MWL high voltage. The slope (in V/s) for the transition to the on-state, as well as the MWL high voltage, are programmed via XTCOS. The same standard voltage limit as for the ACTIVE mode is used for the low MWL voltage ($V_{lim}$).

### Switch off the MWL

Message waiting indication is automatically switched off if an off-hook condition is detected on the line. The line is automatically set to ACTIVE. MWL can also be switched off by setting the line back to ACTIVE mode. Again, the line voltage is first reduced to $V_{lim}$ to guarantee that the lamp is switched off.

## 2.2.14 Overtemperature Detection

The temperature of the DXS is monitored continuously. If the temperature exceeds 145°C, an overtemperature event is generated and the SLIC is switched off to prevent it from being damaged (emergency shutdown). This switching off is reported via an overtemperature event. In emergency shutdown mode, the temperature is still monitored and, if the temperature falls below 125°C, an overtemperature end event is generated.

To filter out spikes on the temperature sensor, debounce counter filtering is performed for the emergency shutdown. To exit from emergency shutdown mode, the channel must be set to DISABLED.

### 2.2.15 Continuous Measurement Function

The DXS allows a number of relevant parameters to be monitored continuously. The following information can be read out:

- Output voltage from DC regulation (Vlim)
- Transversal current (Itrans)
- Ring current of last sent ring burst period (IRing)
- Ring voltage of last sent ring burst period (VRing)
- DC/DC converter lock information
- Charge pump status bit
- DC/DC converter frequency

The value for the output voltage from the DC regulation is calculated from the internally programmed voltage value.

The transversal current is updated every 500 µs as long as the system is in ACTIVE mode. If the values are not updated, then the last measured value is stored. To allow easy interpretation of the measurement in ACTIVE_REVPOL, the transversal current and the output voltage of the DC regulation are inverted, which means that they are reported as a positive value. None of the other values are modified.

The values for the ring current and ring voltage are updated at the end of every ring burst period. When the system is switched to any operating mode other than RINGING, the last measured values are kept. The value of the ring voltage is calculated from the output of the ring voltage regulation. Therefore, it is identical to the programmed ring voltage if no ring voltage regulation is used.

The DC/DC converter lock information, the charge pump bit and the DC/DC converter frequency are updated in all modes.

It is important to note that not all of the values are updated all the time. The updating of the values depends on the operating mode. **Table 5** provides information about how often the values that can be read via the API commands are updated.

**Table 5 Update Values**

| | ACTIVE | RINGING | STANDBY | DISABLED | Message Waiting Lamp |
|---|---|---|---|---|---|
| Vlim | 0.5 ms | No update | No update | No update | No update |
| Itrans | 0.5 ms | 0.5 ms | No update | No update | 0.5 ms |
| IRing | No update | Update every ring period | No update | No update | No update |
| VRing | No update | Update every ring period | No update | No update | No update |
| DC/DC converter lock information | 0.5 ms | 0.5 ms | 0.5 ms[1)] | 0.5 ms[1)] | 0.5 ms |
| Charge pump status bit | 0.5 ms | 0.5 ms | 0.5 ms[1)] | 0.5 ms[1)] | 0.5 ms |
| DC/DC converter frequency | 0.5 ms | 0.5 ms | 0.5 ms[1)] | 0.5 ms[1)] | 0.5 ms |

1) No update in sleep condition

### 2.2.16 SLIC Supply Voltage Generation

The supply voltage of the SLIC is generated and controlled by a DC/DC converter. This converts the available positive supply voltage $V_S$ (typically 12 V) to the negative SLIC supply voltage $V_N$. The integrated control circuitry together with a few external power components (switch transistor, inductor, diode and capacitor) controls $V_N$, ensuring that at any time it equals the minimum possible absolute value. Besides the advantage that, in a DXS-based system, no effort has to be spent designing high voltage supplies, this approach also helps to minimize the power dissipation in any active operating mode, independent of line conditions. Particularly in the most critical ring mode the new concept of quasi-balanced ringing leads to significant on-chip as well as overall system power reduction.

In addition, the DXS offers the possibility to use just one DC/DC converter to generate the voltages required for both channels. This **Combined DC/DC Converter** variant ensures the best possible bill of materials (BOM). Furthermore, a number of DC/DC variants have been developed and tested. These are described in the DC/DC converter application note (see **[12]**). The corresponding reference designs and evaluation boards for these applications are also available (see **[10]**).

Depending on the line status, the following supply voltages are generated:

#### STANDBY

In the STANDBY operating mode, $V_N$ is set to a constant voltage (line voltage $V_{lim}$). As the loop is open, no current and no power has to be fed to the line. To save power, the switching frequency is reduced automatically by reprogramming specific parameters for STANDBY mode. The $V_{lim}$ voltage can be programmed via BBD coefficients.

Off-hook is detected via the power limitation of the DC/DC converter (refer to **Chapter 2.2.10**).

To further reduce power consumption in STANDBY mode, the user can choose one of two predefined fixed voltages: 28 V or 45 V instead of the programmable voltage $V_{lim}$. This feature shall not be selected for combined DC/DC converter solutions. The STANDBY with programmable voltage $V_{lim}$ is the default STANDBY mode. The fixed voltage options can be selected via the XTCOS parameter “Standby Voltage” in the DC characteristics block.

#### ACTIVE

When the phone goes off-hook, a DC path is formed and control loops are activated to meet the programmed DC line characteristic. In this state, the optimum supply voltage is equal to the required DC line voltage plus an additional constant overhead voltage that accounts for the AC signal amplitudes, the internal voltage drop at the output buffer and DC inaccuracies. Through the architecture shown in **Figure 12**, the output voltage $V_N$ is regulated to correspond to the required DC line voltage $V_{TR}$ plus the programmable overhead voltage $V_{OVH}$.

The on-chip power dissipation remains relatively constant, determined predominantly by the overhead voltage $V_{OVH}$ (typically 5 V), and is thus virtually independent of the loop length. This well-known method of line voltage tracking guarantees minimum on-chip power dissipation.

#### RINGING

As explained in detail in **Chapter 2.2.7.3**, ringing is treated in exactly the same way as the normal ACTIVE mode, thus yielding the power-saving quasi-balanced ring signal.

### 2.2.16.1 Basics of DC/DC Operation

**Figure 21** shows the basic topology of the main DC/DC converter application (for other topologies, please refer to **[12]**). A conversion cycle, defined by the period of the switching clock, $1/f_{SW}$, starts by closing switch SW and connecting the inductance $L$ with the positive supply $V_S$. As a consequence, the current in the inductor, $i_L$, rises at the rate $V_S$/L and the capacitor $C$ is discharged by the load current with a time constant of C*$R_L$. After time $t_1$, the current reaches its peak value $I_p = V_S/L*t_1$. Then the switch is opened again and the inductor current decreases at the rate $V_N$/L, i.e. proportional to the output voltage $V_N$. During this time $t_2$ energy is transferred from the inductor to the capacitor and the load, and $C$ is charged again. The ratio of the on-time $t_1$ to the switching period $1/f_{SW}$ is the duty cycle D. For correct operation, D must stay below 0.9. From the converter control dynamics, it is crucial that zero inductor current is reached within each conversion period (discontinuous current mode operation). This means that the total energy stored in the inductor, $L*I_p^2/2$, has been transferred to $C$ and $R_L$, increasing the output voltage by $\Delta V_N$. If this energy is equal to the energy that is dissipated in the load during one conversion cycle, $V_N$ stays constant. This can be achieved by controlling the time $t_1$ and thus the peak current $I_p$ and the transferred energy.

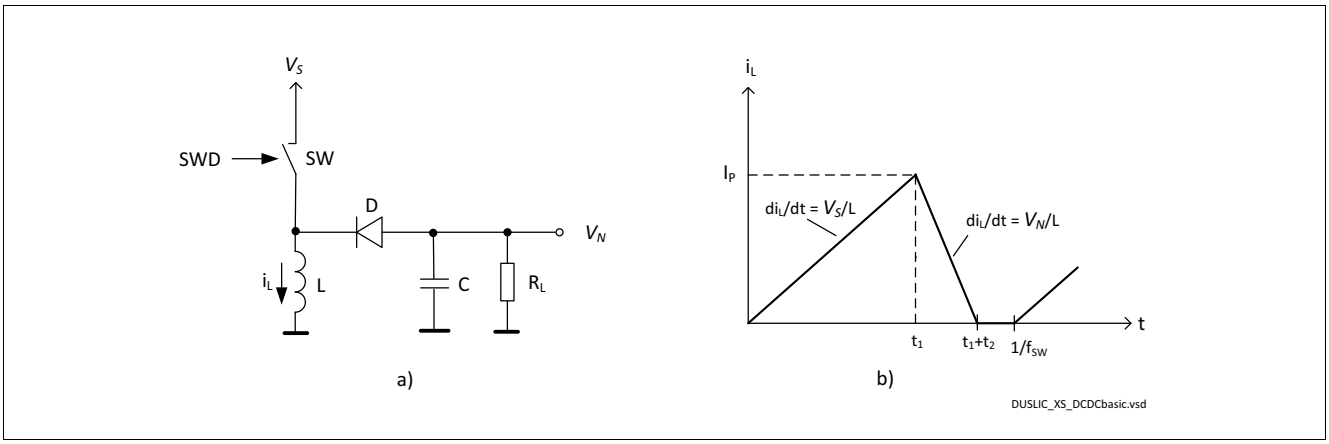


**Figure 21 Inverting Buck-Boost Topology (a) and Inductor Current (b)**

The most important relationships for the dimensioning of the external DC/DC components follow from above. The condition of reaching zero inductor current during any conversion cycle, is equivalent to the discontinuity equation:

$$t_1 + t_2 = I_p * \left( \frac{L}{V_S} + \frac{L}{V_N} \right) < \frac{1}{f_{SW}} \quad (2)$$

The energy transfer condition states that during any conversion cycle the energy stored in the inductor must be equal to the energy dissipated in the load:

$$\frac{L * I_p^2}{2} = \frac{P_{VN}}{\eta * f_{SW}} \quad (3)$$

Here, $P_{VN}$ is the mean load power during a conversion cycle, while the efficiency η accounts for all irregularities and losses. $P_{VN}$ varies strongly depending on the operating mode.

Substituting **Equation (3)** in **Equation (2)** yields an upper limit for the inductance:

$$L < \left( \frac{V_S * V_N}{V_S - V_N} \right)^2 * \frac{\eta}{2 * f_{SW} * P_{VN,\ max}} \quad (4)$$

It should be noted that higher power requires lower inductor values, but from **Equation (3)** this means higher peak currents. In most cases of practical importance, the maximum output power coincides with the maximum output voltage $V_{Nmax}$, that is, the load $R_L$ is ohmic (the US ringer equivalent also forms a nearly ohmic load). With practical $V_{Nmax}/V_S$ ratios of 6 to 10, **Equation (4)** is reduced to:

$$L < 0.7 * \left( \frac{V_S}{V_{N\,max}} \right)^2 * \frac{\eta * R_L}{2 * f_{SW}} \tag{5}$$

Once $L$ is chosen, the peak current, one of the most important parameters for component selection, results from **Equation (3)**.

The concept of ring supply voltage tracking imposes an upper limit on the DC/DC capacitance $C$ due to the d($V_N$)/dt requirements. On the other hand, the voltage change $\Delta V_N$ during each conversion cycle due to charge storage in this capacitance is inversely proportional to $C$. This voltage change is a significant component of the total ripple voltage on $V_N$. Therefore, an additional RC low-pass filter on the output is recommended to smooth $V_N$ sufficiently.

### 2.2.17 Combined DC/DC Converter

The combined DC/DC converter uses only one DC/DC converter to generate the required SLIC supply voltage for both FXS channels. This solution eliminates the need for external components for one of the DC/DC converters, and therefore provides the lowest possible bill of materials.

The SLIC supply voltage needs to be generated in such a way as to fulfill the requirements of both channels, even if one channel can operate at a lower voltage. As a consequence, the total power consumption is higher compared to a dedicated DC/DC converter solution where the voltage can be set individually per channel. Typical power consumption values for different operating modes can be found in chapter “Supply Current and Power Dissipation” of the data sheets **[2]**, **[3]**, **[4]**.

When both channels are operating under the same conditions, the combined DC/DC converter concept requires even less power compared to a dedicated DC/DC converter solution. This is because each DC/DC converter used contributes to part of the total power loss.

In addition there are a number of limitations related to the combined DC/DC converter concept:

- Maximum ringing voltage is 60 $V_{RMS}$ + 15 $V_{DC}$ to limit the power consumption
- Ring current regulation has to be used (e.g. limit ringing current to 30 mA)
- Ring frequency needs to be identical in both channels, for example, it is not allowed to use 20 Hz on channel 0 and 25 Hz on channel 1
- Cadenced ringing is mandatory (power dissipation, heat dissipation)
- No Message Waiting Lamp (MWL) support
- No ground start support

#### 2.2.17.1 Low Power Operation for Combined DC/DC Converter

In the case of the **Combined DC/DC Converter** variant, special low power operation can be activated. This allows the power consumption of the device to be minimized when one channel is in ACTIVE off-hook mode and the other is in STANDBY on-hook mode. This is one of the most critical conditions with respect to power consumption, as the combined DC/DC converter has to supply a high DC voltage for the channel in STANDBY mode while the channel in ACTIVE off-hook mode feeds a DC loop current in the range of 20 mA, which corresponds to a small tip-ring voltage.

The idea is to periodically charge the capacitance on the VN pin of the SLIC for both channels to the maximum required output voltage for a very short time. During the rest of the period the $V_N$ voltage can be reduced to the voltage required for the off-hook channel. Since there is no current flowing in the on-hook channel, the capacitance on the VN pin will only be discharged by the quiescent current of the SLIC.

**Figure 22** shows the tip, ring and $V_N$ voltages for both channels. It is assumed that channel B is in ACTIVE off-hook mode, where the tip and ring wires are constant. The $V_N$ voltage of channel B is always sufficiently high enough to provide the required overhead voltage for AC transmission.

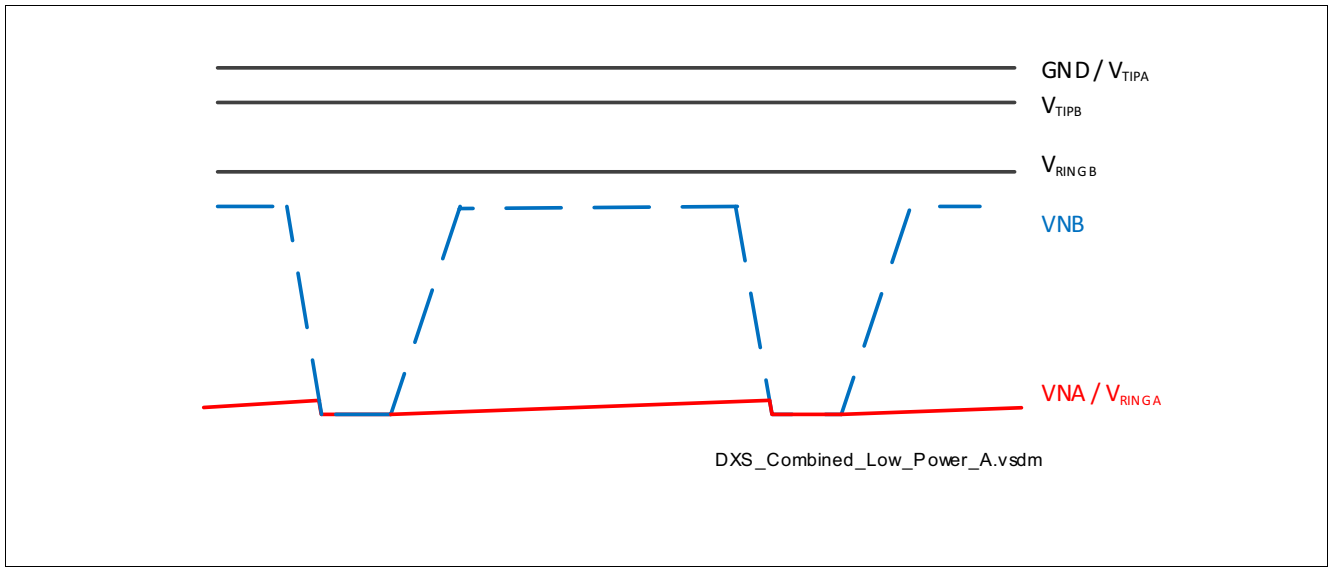


**Figure 22 LP Operation Combined DC/DC - Channel B ACTIVE Off-hook, Channel A STANDBY On-hook**

Channel A is in STANDBY on-hook mode, where the tip wire is connected to ground and the ring wire is connected to $V_N$. It can be seen that the voltage ripple on the ring wire is very low.

This situation changes significantly when the telephone on channel A goes off-hook (see **Figure 23**). The $V_N$ voltage will still be very high during the short charge time, but the voltage $V_{NA}$ will drop for the rest of the period. If it drops by more than CLPOffhook volts for longer than 6 ms, off-hook will be reported and the channel will automatically switch to ACTIVE.

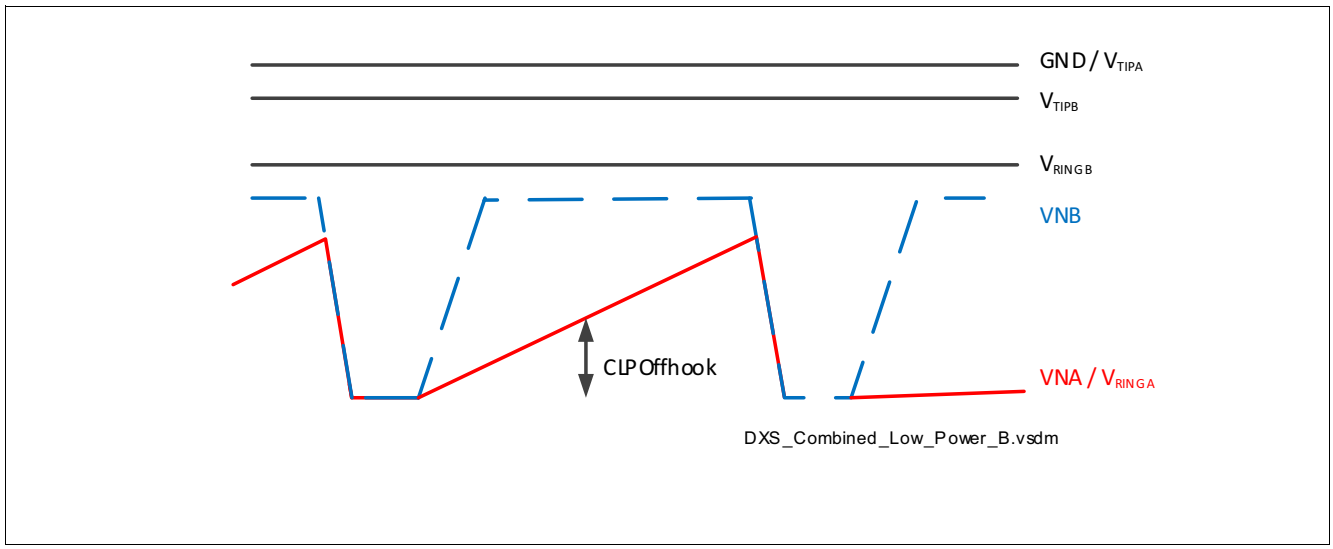


**Figure 23 LP Operation Combined DC/DC - Channel A Goes Off-hook**

The drawback of this method is that there will be a ripple on the ring wire of the STANDBY channel if there is current flowing through the on-hook telephone (e.g. to supply the telephone display). This can be avoided by programming a given overhead voltage CLPOvh (see **Figure 24**).

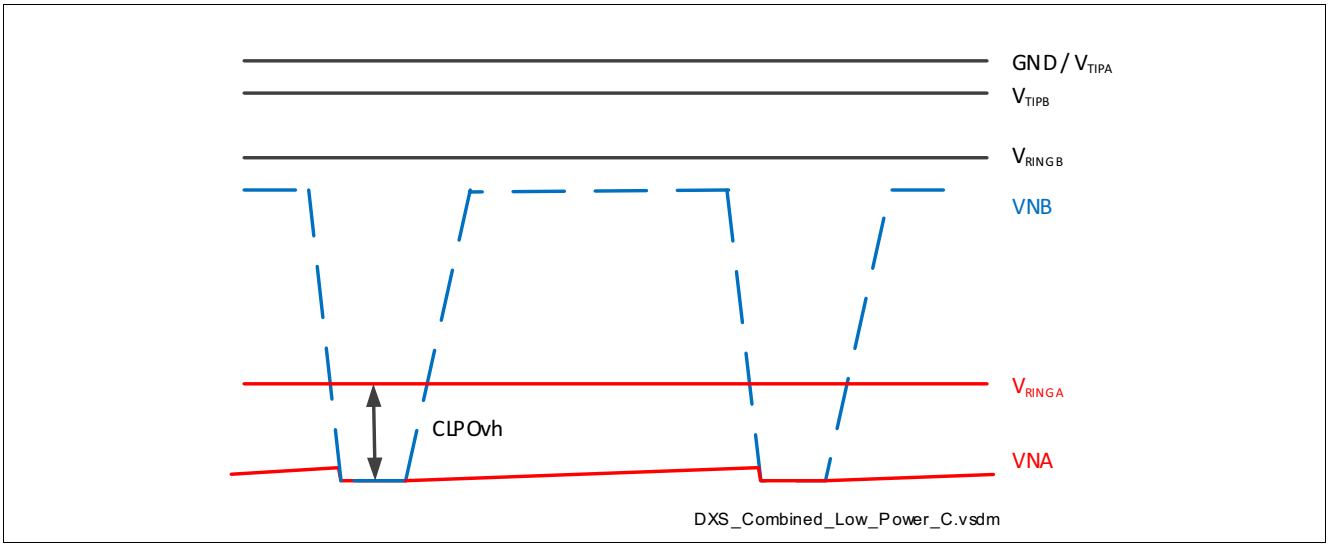


**Figure 24 LP Operation Combined DC/DC - Overhead Voltage Programmed**

During the charge time, $V_N$ will be charged to a voltage that is CLPOvh volts higher (absolute value) than the STANDBY on-hook voltage. Therefore the ring wire of the on-hook channel can be kept constant even if there is a ripple on the $V_N$ supply, as long as the ripple is lower than CLPOvh. Naturally, the power consumption will be higher than for the case where CLPOvh = 0 V as shown in **Figure 22**.

The off-hook detection for the STANDBY channel works as in the previous example. In the case of off-hook, the voltage on the ring wire will also drop (see **Figure 25**). If it drops below the CLPOffhook threshold for longer than 6 ms, off-hook will be reported and the channel will automatically switch to ACTIVE.

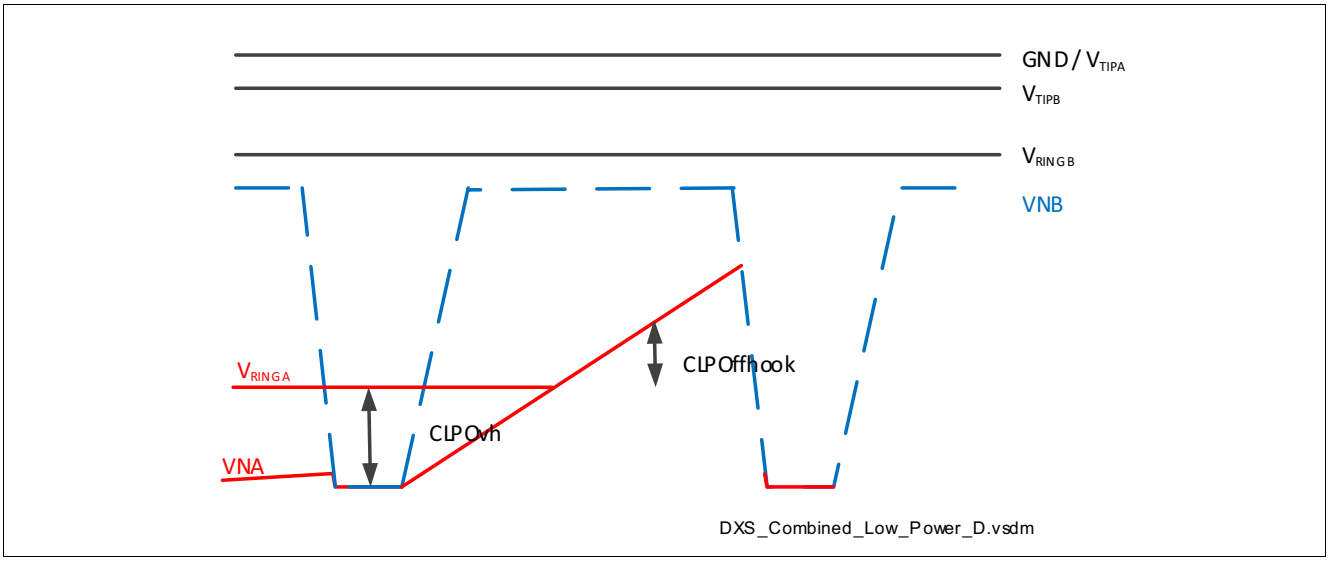


**Figure 25 LP Operation Combined DC/DC - Off-hook Detection with Overhead Voltage Programmed**

This feature can be enabled within the "Low Power Features" in XTCOS, provided that a combined DC/DC converter module has previously been selected, see **Figure 14**.

To achieve the lowest possible power consumption, CLPOvh shall be set to 0 V and the CLPOffhook threshold shall be set to 15 V as shown in **Figure 22**.

For on-hook currents of up to 3 mA, CLPOvh shall be set to 15 V and the CLPOffhook threshold shall be reduced to 5 V as shown in **Figure 24**. For higher on-hook currents, the "Combined Low Power" settings shall be disabled.

## 2.3 Tone Generation and Detection

### 2.3.1 Tone Generation (Controller)

The tone management API functions of the DXS Device Driver allow for the generation of up to two fully flexible programmable tones (frequency, level) that can either be added or amplitude modulated.

#### 2.3.1.1 DTMF/AT Generator

Dual Tone Multi-Frequency (DTMF) is a signaling scheme using voice frequency tones to signal dialing information and works according to ITU-T Q.23. A DTMF signal is the sum of two tones, one from a low group (697 ... 941 Hz) and one from a high group (1209 ... 1633 Hz), with each group containing four individual tones. This scheme allows sixteen unique combinations. Ten of these codes represent the numbers on the telephone keypad from zero to nine. The remaining six codes (*, #, A, B, C, D) are reserved for special signaling. The buttons are arranged in a matrix, with the rows determining the low group tone and the columns determining the high group tone for each button.

The chip internal DTMF/AT generator can generate the sixteen standard DTMF tone pairs, alert tones or any other single-frequency or dual-frequency tones. The generated DTMF tone signals meet the frequency variation tolerances specified in the ITU-T Q.23 recommendation **[20]**.

The DTMF signal is sent to the line. It can optionally overlay the PCM data in RX as shown in **Figure 26**.

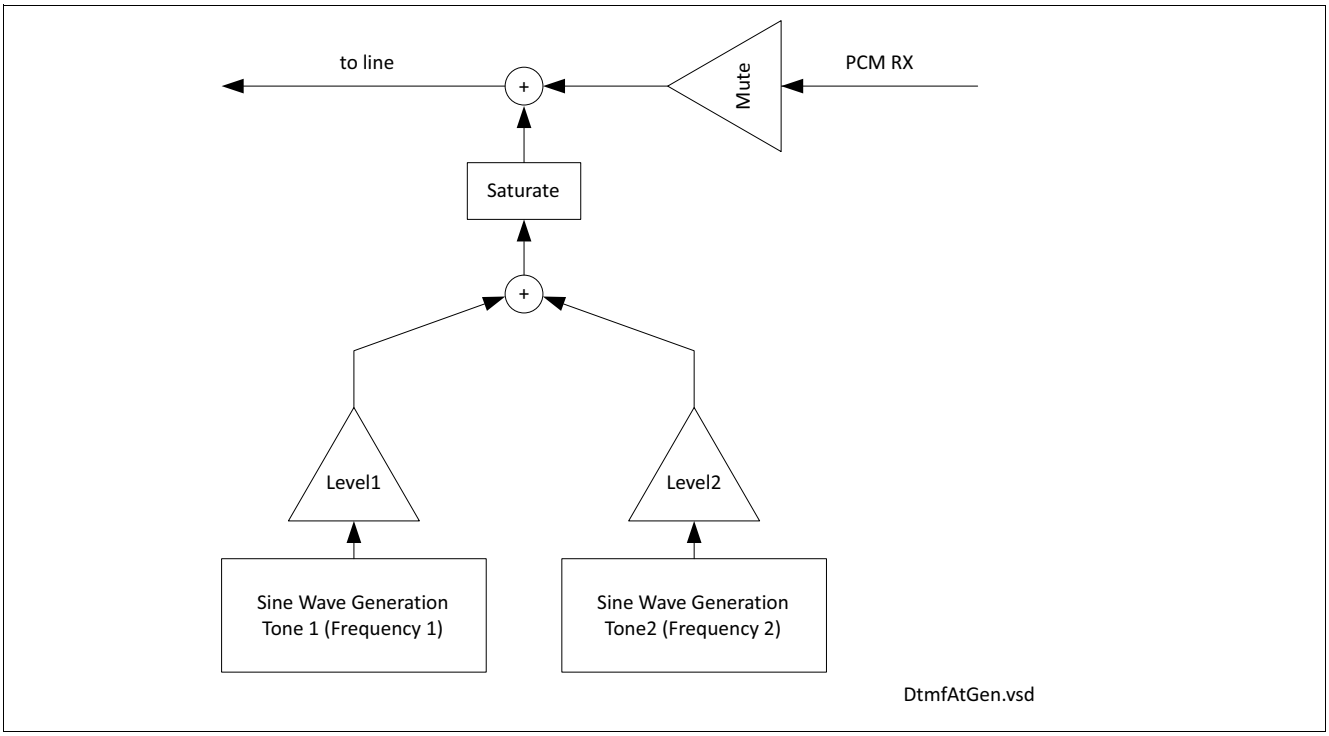


**Figure 26 DTMF Generation, PCM Adder in RX (Digital to Analog) Direction**

The new tone generator implementation also allows the modulation of tone 1 with tone 2 (amplitude modulation), where tone 1 is the signal carrier, tone 2 relates to the modulation frequency and the level configures the modulation index (see **Figure 27**).

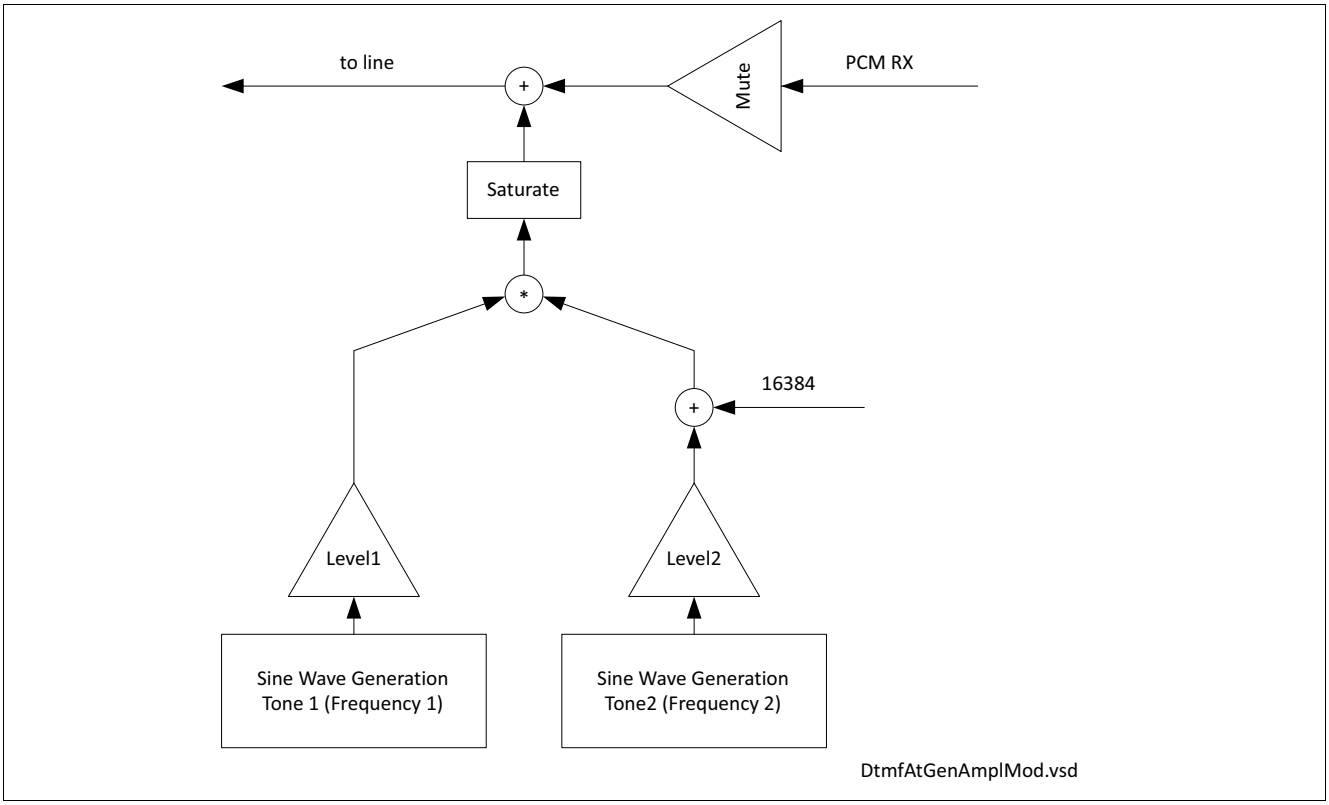


**Figure 27 Amplitude Modulation of DTMF or Alert Tone**

### Programming

The services required to configure and control the tone generators are provided by the DXS Device Driver.

## 2.3.2 DTMF Receiver

The DTMF receiver (also called DTMF detector) can be switched off individually for each channel to reduce power consumption. In normal operation, the receiver monitors the transversal current on the line (transmit path).

As soon as the DTMF receiver detects a valid DTMF sign, it signals this to the device driver.

The behavior of the DTMF receiver when a valid tone has been detected followed by a pause < 20 ms:

- If the pause is followed by a tone pair with the same frequencies as before, this is interpreted as drop-out.
- If the pause is followed by a tone pair with different frequencies and if all other conditions are valid, the second tone pair is interpreted as a newly dialed digit.

### DTMF Receiver Performance Characteristics

The receiver algorithm complies with the requirements of the ITU-T Q.24 and Bellcore GR-30-CORE (TR-NWT-000506) standards, and of the Deutsche Telekom network (BAPT 223 ZV 5, Approval Specification of the Federal Office for Post and Telecommunications, Germany), among others. The DTMF decoder also has excellent speech rejection capabilities and complies with Bellcore TR-TSY-000763. The algorithm has been tested fully with the speech sample sequences in the Series-1 Digit Simulation test tapes for DTMF decoders from Bellcore. **Table 6** shows the performance characteristics of the DTMF decoder algorithm.

**Table 6 Performance Characteristics of the DTMF Receiver Algorithm**

| Characteristic | Value | Remark |
|---|---|---|
| Valid input signal detection level | -40 to 0 dBm0 | – |
| Input signal rejection level | -5 dB of valid signal detection level | – |
| Positive twist accept | < 8 dB | – |
| Negative twist accept | < 8 dB | – |
| Frequency deviation accept | < ±(1.5% + 4 Hz) and < ±1.8% | Related to center frequency |
| Frequency deviation reject | > ±3% | Related to center frequency |
| DTMF noise tolerance | -12 dB | dB referenced to lowest amplitude tone |
| Minimum tone accept duration | 40 ms | – |
| Maximum tone reject duration | 25 ms | – |
| Signaling velocity | ≥ 93 ms/digit | – |
| Minimum inter-digit pause duration | 40 ms | – |
| Maximum tone drop-out duration | 20 ms | – |
| Interference rejection 30 Hz to 480 Hz for valid DTMF recognition | Level in frequency range 30 Hz … 480 Hz ≤ level of DTMF frequency +22 dB | dB referenced to lowest amplitude tone |
| Gaussian noise influence signal level -22 dBm0, SNR = 23 dB | Error rate better than 1 in 10000 | – |
| Pulse noise influence impulse noise tape 201 according to Bellcore TR-TSY-000762 | Error rate better than 14 in 10000 | Measured with DTMF level -22 dBm0 Impulse Noise -10 dBm0 and -12 dBm0 |

**Programming**

The services required to configure and control the tone generators are provided by the DXS Device Driver.

## 2.3.3 Caller ID Support

A chip internal Caller ID generator supports FSK modulation according to ITU-T V.23 [23] or Bell 202. After enabling the Caller ID generator and sending the first data byte, the CID sender starts the transmission by automatically sending the channel seizure and mark sequence.

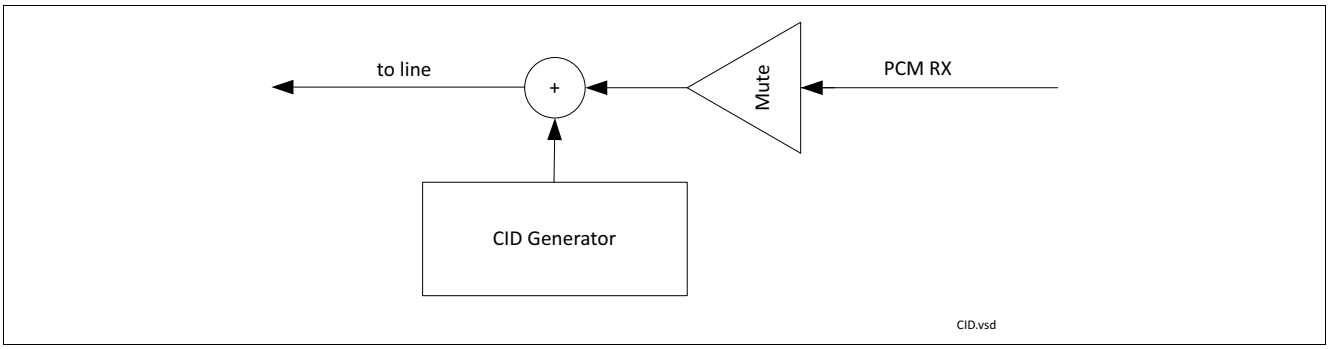


**Figure 28 CID and PCM Data Stream**

The CID signal is sent to the line. It can optionally overlay the PCM data in RX as shown in **Figure 28**.The example in **Figure 29** shows the signaling of a CID on-hook data transmission in accordance with Telcordia **[25]** specifications. In this case, the Caller ID information applied on tip and ring is sent during the period between the first and second ring burst. The CID module supports the C, D and E phase.

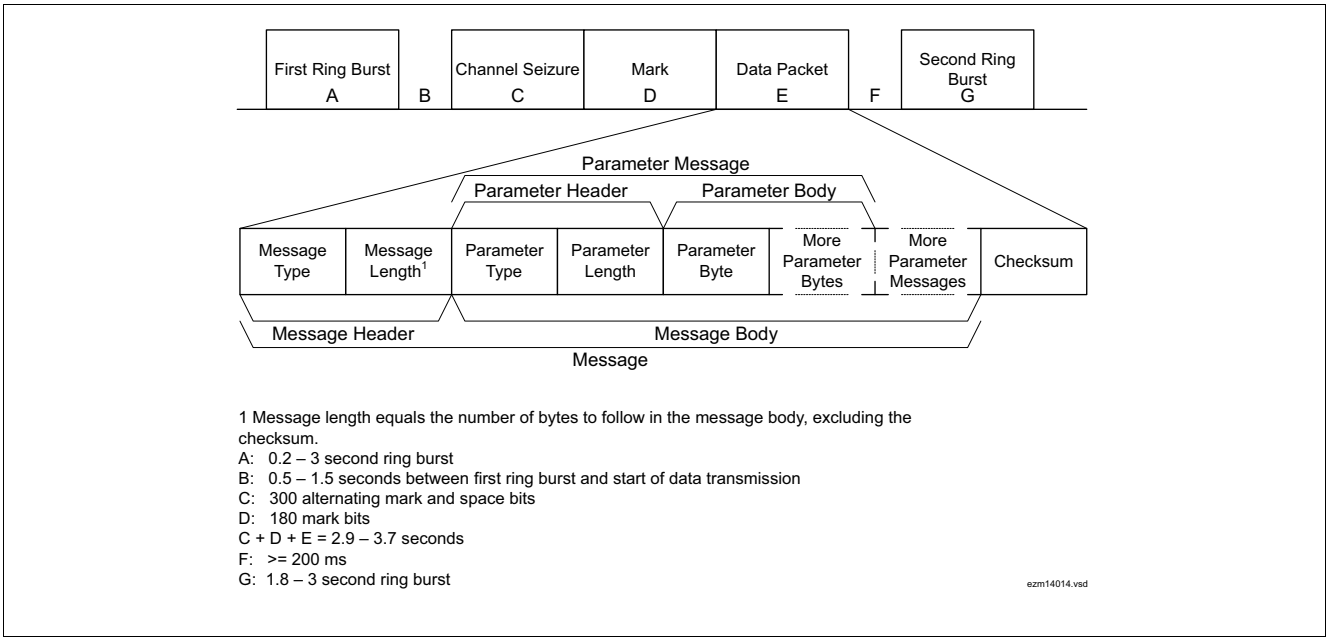


**Figure 29 Bellcore On-hook Caller ID Physical Layer Transmission**

The following transmission features are supported:

- Caller ID with on-hook transmission associated with power ringing (Caller ID type 1).
- Caller ID with on-hook transmission not associated with power ringing (Visual Message Waiting Indication).
- Caller ID with off-hook transmission (Caller ID type 2).
- Support for additional Analog Display Service Interface (ADSI) (Caller ID type 3).

World wide Caller ID signaling standards are supported by the DXS Device Driver at a higher level. The Caller ID features refer to the following standards:

- Telcordia **[25]**
- ETSI **[18]** - implementing FSK coding, data transmission during ringing and all defined data transmissions prior to ringing (Dual Tone AS, Ring Pulse AS and Line Reversal followed by Dual Tone AS).
- British Telecom (BT) **[17]**
- NTT **[24]**

### 2.3.4 Universal Tone Detector (UTD)

The UTD detects a tone that lies within a configurable frequency range. If a tone consisting of two different frequencies has to be detected, then both frequencies must lie within the configured frequency range.

In addition to the frequencies, the detection level and the rejection level can be configured. The tone must be stable for a minimum configurable time duration to allow the tone detection to be reported.

The UTD can be configured to detect tones in the upstream and downstream directions. The UTD coefficients have to be calculated using XTCOS before the UTD can be used.

## 2.4 DXS Integrated Testing Features

The DXS offers three groups of integrated testing features. Two of them, the Signaling Tests and the AC Level Meter require a given resistive termination (for example, 600 Ω) to be connected by means of relays, which can be controlled via any free GPIO pins. The three groups of testing features are:

- **Enhanced GR-909 Tests (Test-Out condition)**
  This group of tests is used to monitor the home wiring and CPE terminations, as shown by the Test-Out (open) condition in **Figure 30**. The standard GR-909 tests and capacitance measurements are available in the DXS API Library.
- **Signaling Tests (Test-Out and Test-In condition)**
  This group of tests allows verification of the complete signal transmission and processing between the host and the CPE. The pass/fail criteria have to be implemented in the customer's application software, elaborating the sequence of events detected by the remote DXS located in the CPE.
- **AC Level Meter (Test-In condition)**
  This group of tests is used to test the DXS voice transmission quality. This is achieved by connecting a dedicated test load (for example, 600 Ω) between the tip and ring wires, as shown by the Test-In (closed) condition in **Figure 30**. This resistance may be in parallel to any other loop termination, such as a telephone or signature, whenever connected. For example, when an on-hook telephone terminates the loop, the test load is parallel to an impedance of a few kΩ. Conversely, if the loop is open on the CPE side, the 600 Ω resistance is the only load on the DXS FXS port in the Test-In condition. This feature can also be used in the CPE set-top box or home gateway production and testing phase, where it is necessary to terminate the FXS port with a known resistive load.

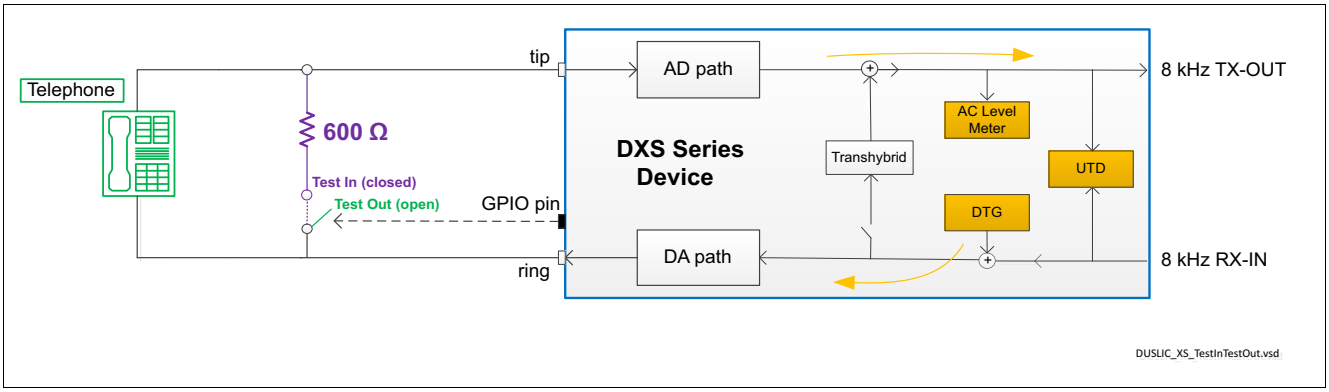


**Figure 30 DXS Test-In and Test-Out Conditions**

The DXS test list is provided in **Table 7**.

**Table 7 DXS Test List**

| Tests | | Condition | Failures / Test Coverage / Benefits |
|---|---|---|---|
| **Enhanced GR-909 Test Suite** | | | |
| Standard GR-909 Tests | Hazardous Potential | Test Out | Line faults |
| | Foreign Electromotive Force | | Line faults |
| | Resistive Fault | | Line faults |
| | Receive Off-Hook | | CPE off-hook state detection |
| | Ringer Impedance | | CPE on-hook state detection |
| Capacitance Test | | | Line faults, wiring error, CPE termination |
| Phone Detection Test | | | CPE termination detection |
| **Signaling Tests** | | | |
| Make-and-Break Dial Tone | | Test In | Off-hook detection<br>Dial tone detection (make)<br>DTMF or pulse dialing<br>End of dial tone detection |
| Universal Tone Detection (UTD) Test | | Test In/Out | Tone detection (e.g. ring back tone)<br>DTMF detection<br>End of tone detection |
| **AC Level Meter** | | | |
| AC Transhybrid Loss | | Test In | Voice band echo |
| AC Frequency Response | | | Voice transmission quality |
| AC Gain Tracking | | | Voice transmission quality |
| AC SNR | | | Voice transmission quality |

### 2.4.1 Enhanced GR-909 Tests

Telephone lines can be affected by a number of typical fault conditions, such as foreign voltage connection or interference, leakage resistance to either ground potential or between the ring and tip wires, or too many or no phones connected (see **Figure 31**). In addition, the wiring on the CPE side might be wrong. It is important that such conditions are detected in order to help the customer achieve a correct installation.

The GR-909 Tests have to be performed in the **Test-Out condition**.

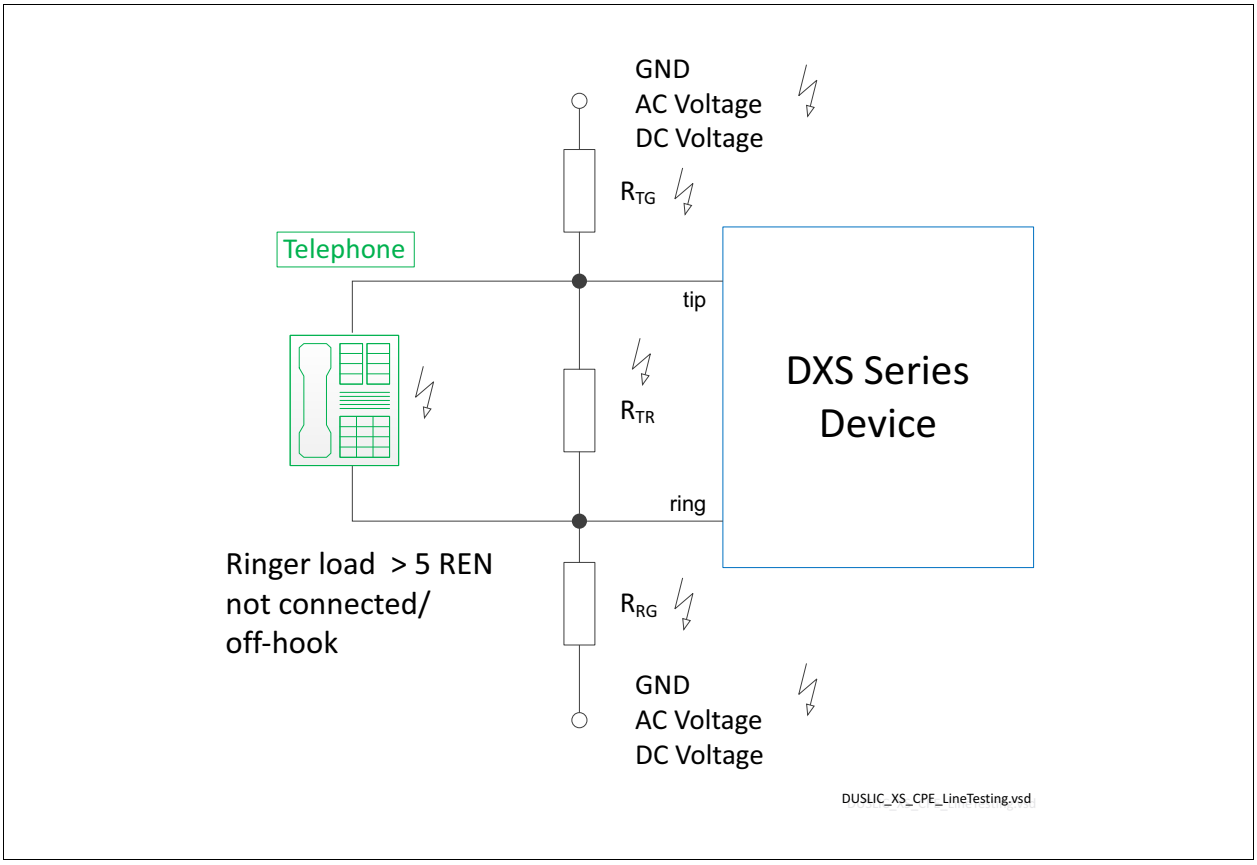


**Figure 31 Common Faults on Subscriber Loops**

#### 2.4.1.1 Standard GR-909 Tests

GR-909 ([26]) defines a set of metallic line testing functions to check for common faults on a POTS line. These functions are:

- **Hazardous Potential Test (HPT)**
  This test checks for high voltage levels on the line. A hazardous potential means an overvoltage detected between the tip and ring wires, the tip wire and ground, or the ring wire and ground.
- **Foreign Electromotive Force (FEMF) Test**
  This test checks for excess voltage on the line. The FEMF test detects an excessive voltage between the tip and ring wires, the tip wire and ground, or the ring wire and ground.
- **Resistive Faults Test (RFT)**
  This test checks for resistive (DC resistance) faults between the tip and ring wires (shorts), the tip wire and ground, and the ring wire and ground (grounds). The test fails when the resistance value is too low.
- **Receiver Off-hook (ROH) Test**
  The ROH test distinguishes between a tip and ring resistive fault and an off-hook condition. A receiver off-hook (ROH) can be identified by several means. For example, ROH can be determined by measuring the tip to ring DC resistance at two different test voltage levels, and looking for a non-linear relationship in the DC resistance.
- **Ringer Test (RIT)**
  This test determines the presence of appropriate ringer terminations on the customer's line.

The channel under test must first be set to DISABLED mode. Then all five tests are executed in a sequence by setting the operating mode to GR909. The DISABLED mode is automatically restored after the measurement is finished. The full GR-909 test sequence takes a maximum of two seconds. The pass criteria and test outputs are described in detail in Table 8. The results can be read out using the API function DxsGR909ResultGet.

**Table 8 GR-909 Test Pass Criteria and Test Outputs**

| | Test Details | |
|---|---|---|
| **Hazardous Potential Test (HPT)** | | |
| Pass criteria | $V_{RMS}$ AC | $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ < 50 V |
| | V DC | $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ < 135 V |
| Measurement range & accuracy[1)] | $V_{RMS}$ AC | Range: 0 - 230 $V_{RMS}$<br>Accuracy: 10% ±1 V |
| | V DC | Range: 0 - 325 V<br>Accuracy: 10% ±2 V |
| Output flags | HPT Pass/Fail<br>HPT Valid/NotValid | |
| **Foreign Electromotive Force (FEMF) Test** | | |
| Pass criteria | $V_{RMS}$ AC | $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ < 10 V |
| | V DC | $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ < 6 V |
| Measurement range & accuracy[1)] | $V_{RMS}$ AC | Range: 0 - 230 $V_{RMS}$<br>Accuracy: 10% ±1 V |
| | V DC | Range: 0 - 325 V<br>Accuracy: 10% ±2 V |
| Output flags | FEM Pass/Fail<br>FEM Valid/NotValid | |

**Table 8 GR-909 Test Pass Criteria and Test Outputs** (cont'd)

| | **Test Details** |
|---|---|
| **Resistive Faults Test (RFT)** | |
| Pass criteria | $R_{T-G}$, $R_{R-G}$, $R_{T-R}$ > 150 kΩ |
| Measurement range & accuracy[1)] | Range: 0 - 3 MΩ<br>Accuracy for values up to 1 MΩ: 10% ±5 Ω<br>Accuracy for values ≥ 1 MΩ: 20% |
| Output flags | RFT Pass/Fail<br>RFT Valid/NotValid |
| **Receiver Off-hook (ROH) Test** | |
| Pass criteria | Test $ROH_{T-R}$ 1 in "receiver off-hook" condition<br>Test $ROH_{T-R}$ 2 in "receiver off-hook" condition<br>$ROH_{T-R}$ 1 and $ROH_{T-R}$ 2 must be measured with different test voltages.<br>→ Delta between $ROH_{T-R}$ 1 and $ROH_{T-R}$ 2 must be lower than 15% |
| Measurement range & accuracy[1)] | Range: 0 - 1048 kΩ<br>Accuracy: 10% ±16 Ω |
| Output flags | ROH Pass/Fail<br>ROH Valid/NotValid |
| **Ringer Impedance Test (RIT)** | |
| Pass criteria | Test of ringing impedance RI at ringing frequency (typ. 25 Hz).<br>RI should be in the range: 1.4 kΩ < RI < 40 kΩ<br>This is equivalent to testing the Ringer Equivalent Number REN<br>(1 REN = 6930 Ω in series with 8 µF according to FCC 68.312 part),<br>that is: 0.175 < REN < 5 |
| Measurement range & accuracy[1)] | Range: 0 - 1048 kΩ<br>Accuracy: 10% ±16 Ω |
| Output flags | RIT Pass/Fail<br>RIT Valid/NotValid |

1) The accuracy refers to single component measurements, that is, measurements where just one external component or foreign voltage is connected at once. The accuracy specification only applies for standard ambient temperature and supply conditions. It does not apply if the result is marked as NotValid via the validity flag.
It is recommended that Open Loop Calibration is executed in order to meet the accuracy targets of **Table 8** and **Table 10**, in particular for resistances >500 kΩ and capacitances <100 nF, see also **Chapter 2.4.2**.

**Figure 32** shows the flow chart for the GR-909 measurements and indicates which measurements are executed or skipped when failures occur.

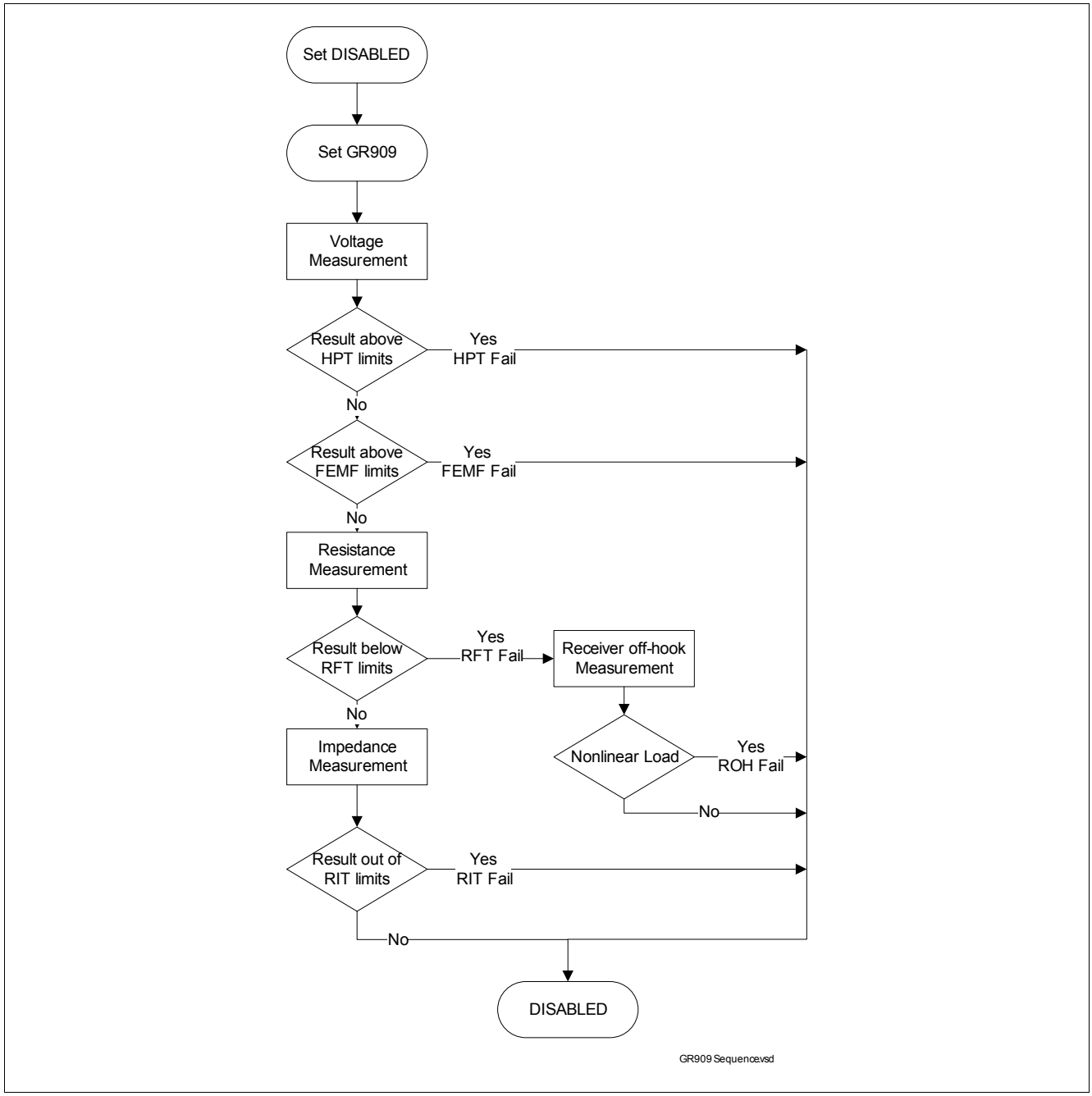


**Figure 32 GR-909 Test Sequence Flow Chart**

Table 9 describes how a given failure may be recognized from the GR-909 line testing results.

**Table 9 GR-909 Tests - Failure Causes**

| Test | Faulty Test Result | Possible Cause of Failure |
|---|---|---|
| HPT | AC: $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ > 50 V | Power contact with the 110-230 V main power line.<br>Power contact with a generic AC source.<br>Coupling with other POTS wire (ringing signal). |
| FEMF | AC: $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ > 10 V | Coupling with a generic small AC source. |
| HPT | DC: $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ > 135 V | Power contact with DC source, battery voltage.<br>Coupling with another POTS wire (DC Feeding). |
| FEMF | DC: $V_{T-G}$, $V_{R-G}$, $V_{T-R}$ > 6 V | Coupling with a generic small DC source. |
| RFT | $R_{T-G}$, $R_{R-G}$, $R_{T-R}$ < 150 kΩ | Resistive fault, ground fault:<br>Tip or ring or both wires are connected to ground, short between tip and ring.<br>Leakage resistance due to humidity or corrosion. |
| ROH | Delta between $ROH_{T-R}$ 1 and $ROH_{T-R}$ 2 > 15% | Phone(s) accidentally left off-hook. |
| RIT | RI > 40 kΩ | No ringer (on-hook phone) connected.<br>Phone ringer circuit damaged.<br>FXS connector (RJ) damaged.<br>Tip or ring wire broken.<br>Wrong home wiring. |
| RIT | RI < 1.4 kΩ | Too many on-hook phones in parallel.<br>Small generic AC impedance terminating the loop. |

### 2.4.1.2 Capacitance Measurement

In addition to the GR-909 line testing measurements, the DXS allows measurement of the capacitance values from tip to ring (Ctr), tip to ground (Ctg) and ring to ground (Crg). The measurement is started by setting the operating mode to **CAP_MEAS**, provided the initial operating mode is DISABLED as for the GR-909 test sequence, see **Chapter 2.2.4.** The results can be retrieved using the API function **DxsCapMeasurementResultGet**.

The capacitance measurement range is up to 10 µF, with accuracy 5% ±5 nF[1)]

It is recommended that open loop calibration is executed before performing any capacitance or resistance measurements in order to optimize the accuracy of the measurements, see **Chapter 2.4.2 Open Loop Calibration (OLC)** for further details.

1) The accuracy refers to single component measurements, that is, measurements where just one external component or foreign voltage is connected at a time. The accuracy values apply for standard ambient temperature and supply conditions.

### 2.4.1.3 Phone Detection Test via Capacitance Measurement

As described in **Chapter 2.4.1**, the GR-909 test feature includes a ringer test that measures the ringer load of a connected telephone. This test is optimal for traditional ringer loads, and especially for the detection of mechanical ringers. However, it is possible that telephones with electronic ringers might not be detected by the GR-909 ringer test.

To overcome this problem, the DXS allows telephones with electronic ringers to be detected using capacitance measurements. The capacitance measurement is optimized to detect telephones with small capacitances between the tip and ring wires. The threshold should be high enough to ensure that there is no confusion with the wiring capacitance in the case of an on-hook phone. An example is described in **Table 10**.

The phone detection test can be implemented in the customer application software. The recommended test sequence consists of the following tests:

- Check if the phone is in the off-hook state at the start of the test. If yes, the capacitance test is skipped.
- Detect whether an on-hook phone is connected by means of a tip to ring capacitance measurement.
- Check if the capacitance to ground is normal or abnormal.

Examples of pass criteria and test outputs are described in detail in **Table 10** and **Table 11**.

**Table 10 Phone Detection Test Pass Criteria and Test Outputs**

| | **Test Details** |
|---|---|
| Pass criteria | If Ctr > 50 nF (example), phone detection is pass.<br>If Ctg and Crg < 20 nF[1)] (example), capacitance to ground is normal. |
| Measurement range & accuracy[1)] | Range: 0 - 10 µF<br>Accuracy: 5% ±5 nF |
| Test output | Phone Detection Pass/Fail<br>Capacitance to Ground Pass/Fail |

1) The value of 20 nF is given as an example. In general, this value should correspond to the expected maximum home wiring loop length, with some tolerance to allow for factors such as the real cable parameters.

**Table 11** describes how a given failure may be recognized from the phone detection test results.

**Table 11 Phone Detection Test - Failure Causes**

| **Test** | **Faulty Test Result** | **Possible Cause of Failure** |
|---|---|---|
| | Ctr < 50 nF[1)] | No ringer (on-hook phone) connected.<br>Tip or ring wire broken or left open.<br>Wrong wiring. |
| | Ctg > 20 nF or Crg > 20 nF[2)] | Coupling with another POTS line.<br>Phone ringer damaged and short circuited to ground. |
| | Off-hook condition at the start of the test | Short circuit between tip and ring, low ohmic resistance between tip and ring.<br>FXS connector is accidentally shortened by home wiring. |

1) The threshold of 50 nF can be modified depending on the typical lowest phone capacitance value.

2) The threshold value of 20 nF is given as an example. In general, this value should correspond to the expected maximum home wiring loop length, with some tolerance to allow for factors such as the real cable parameters.

### 2.4.2 Open Loop Calibration (OLC)

During the **Standard GR-909 Tests** and **Capacitance Measurement**, the test sequence is not only influenced by the external network but also by some of the channel-specific DXS external components. For example, until the open loop calibration[1)] is executed, the capacitance measurement results Ctg and Crg include the capacitance $C_{STAB}$ in parallel, that is an offset of typically 15 nF. Assuming the $C_{STAB}$ components have a tolerance of 10%, subtracting only the nominal value from the measurement results can add an additional channel-specific error. Therefore, it is far more efficient to calibrate the Ctg, Crg and Ctr results using channel-specific values that can be measured in the open loop condition.

A similar channel-specific error originates from the voltage sense resistors $R_M$, 1.5 MΩ nominal value. These components are in parallel with each tip to ground, and ring to ground resistance to be measured. In this case, the DXS firmware automatically subtracts the $R_M$ in parallel from the total Rtg and Rrg measured values, but a resistance error due to the tolerance of $R_M$ and the non-linearity of the current sensor still remains. This error (a kind of virtual parallel resistance) can only be compensated by means of a channel-specific open loop calibration, which can be performed during the production phase of the CPE system that includes the DXS (factory calibration).

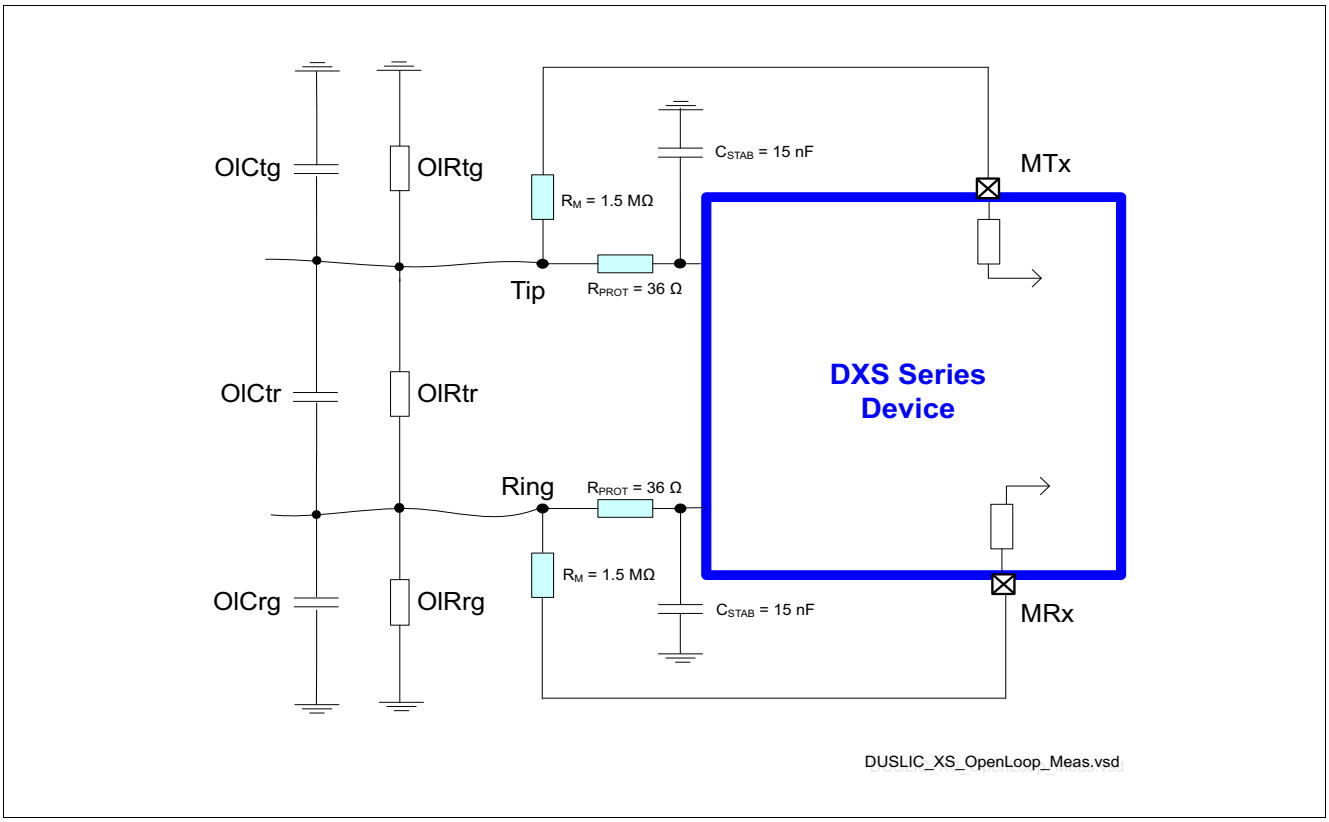


**Figure 33 Virtual Calibration Results and External Components**

#### Open Loop Calibration (Factory Calibration)

The Line Testing Library offers an API function to perform the open loop calibration: **DxsOpenLoopCalibration**. The result of the open loop calibration is a set of three virtual conductances and three virtual capacitances that appears to be physically connected to the chip as an external six-element load, refer to **Figure 33**. The OICtg, OICrg and OICtr values are measured with the **Capacitance Measurement**, see also **Figure 34**. In order to

1) The open loop Calibration described in this chapter has nothing to do with the CALIBRATION mode described in **Chapter 2.2.4 Operating Modes**. The CALIBRATION mode is used for internal offset compensation only.

reduce the measurement noise, the **DxsOpenLoopCalibration** API is able to repeat the measurement several times (programmable parameter) and to calculate the average values.

The three virtual conductances OlGtg, OlGrg and OlGtr are calculated by the **DxsOpenLoopCalibration**[1)] API and returned via three output values in the range 0 to 255.

At the end of the factory calibration process, the six channel-specific calibration results (3 capacitances and 3 conductances) have to be stored in dedicated memory on the CPE board by means of the customer application. They are then available for each future field measurement.

### Open Loop Calibration for Device Evaluation Tests

For simple evaluation tests in the laboratory, it is not mandatory to have performed the open loop calibration before, as it is always possible to disconnect the tip and ring wires from any external load. In this case, it is sufficient to call the **DxsOpenLoopCalibration** API for each channel; the DXS will then be ready for calibrated GR-909 tests and capacitance measurements.

### Field Measurements

It is recommended that each line testing measurement is processed using the results of the open loop calibration. In order to do this, the customer application has to read the six stored open loop calibration values during system startup, before any line testing operation is executed. Afterwards, the API function **DxsOpenLoopConfigSet** can be used to supply these values to the Line Testing Library.

The final correction and saturation of the GR-909 resistance and capacitance results takes place in the corresponding get functions: **DxsGR909ResultGet** and **DxsCapMeasurementResultGet**.

Final resistance results greater than 3 MΩ will be saturated to 3 MΩ, while the final negative capacitance values will be saturated to 0 nF.

### Line Testing with Default OLC Values

It is also possible, but not recommended, to use line testing functions with default open loop calibration values, that is, without running the open loop calibration at all. In this case, the accuracy of high ohmic resistances (> 500 kΩ) or small capacitance measurements (<100 nF) is reduced depending on how far the default values match the channel under test. The default open loop calibration values (reset values) are the following:

- Ctg = Crg = 15
- Ctr = 7
- Gtg = Grg = 51
- Gtr = 48

The Ctg, Crg and Ctr open loop values are expressed in nanofarad (nF). Ctg and Crg correspond to the standard external Cstab capacitors of 15 nF each, connected between tip to ground and ring to ground. The Ctr value is basically the series of two 15 nF capacitors, rounded to a value of 7 nF.

The Gtg, Grg and Gtr default values are decimal values which can be calculated from the typical open loop resistances tip-ground, ring-ground and tip-ring accordingly by the following formulas:

Gtg = Grg = round($(2^{16} * 1158) / (1.5 * 10^6)$)

Gtr = round($(2^{19} * 1158) / (12.6 * 10^6)$)

The 1.5 MΩ correspond to the standard external $R_M$ measurement resistors (Tip-Ground, Ring-Ground), while 12.6 MΩ is the typical internal Tip-Ring leakage resistance which is always in parallel to the external Tip-Ring load.

*Note: Open loop calibration values can be reused after a software update. There is no need to run the OLC process again after a software update or reset.*

1) This API first of all resets all the default open loop values; afterwards it searches for the optimal channel specific values by means of N calibration iterations, for both the open loop capacitances and conductances.

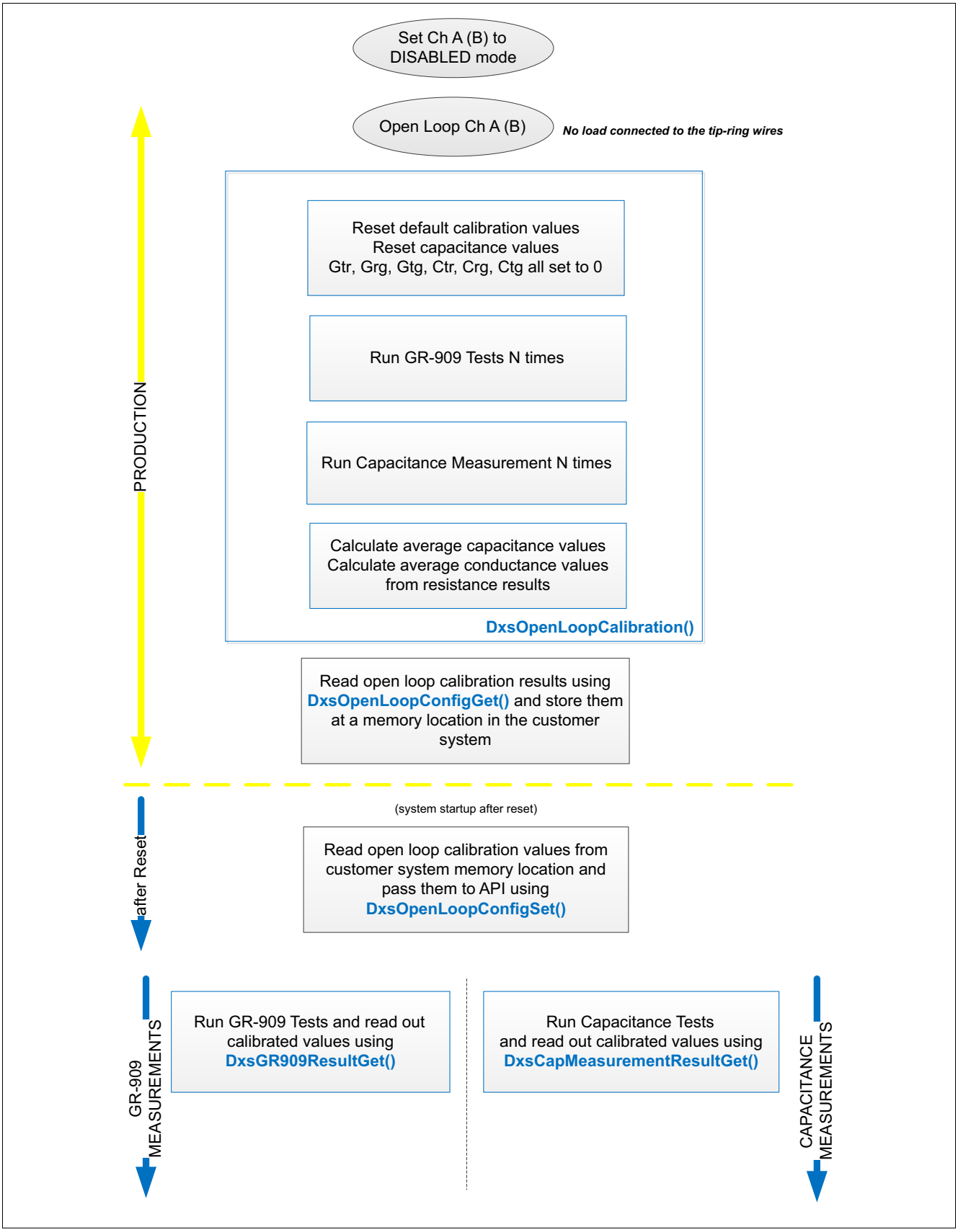


**Figure 34 Open Loop Calibration Flow**

### 2.4.3 Signaling Tests

This group of tests allows verification of the complete signal transmission and processing between the host and the CPE.

#### 2.4.3.1 Make-and-Break Dial Tone Test

The goal of this test is to measure the following parameters:

- Time between an off-hook event and the application of a dial tone to the line → MAKE
- Time between a dial event and the removal of the dial tone from the line → BREAK

This test is also known as the “draw-and-break” dial tone test. It can be performed with or without a phone connected to the selected channel as the off-hook is generated by an external test switch, connected to the DXS GPIOs, which switches a 600 Ω resistance between the tip and ring lines. The pass criteria and test outputs are described in detail in **Table 12**.

**Test Description**

The test can be implemented in the customer application software using the DXS API Library functions. The recommended test sequence consists of the following steps:

- Self off-hook generation by switching 600 Ω between tip and ring
- Dial tone start detection
- Pulse dialing emulation of a given digit
- Pulse digit detection
- Dial tone stop detection

**Table 12 Make-and-Break Dial Tone Test Pass Criteria and Test Outputs**

| | Test Details |
|---|---|
| Pass criteria | Pass/fail criteria have to be implemented in the customer’s application layer, according to the customer’s own specification. |
| Test output | The DXS will provide the following signaling events:<br>off-hook detection, dial tone start detection, pulse digit detection, dial tone stop detection |

**Table 13** describes how a given failure may be recognized from the make-and-break dial tone test results.

**Table 13 Make-and-Break Dial Tone Test - Failure Causes**

| Test | Faulty Test Result | Possible Cause of Failure |
|---|---|---|
| | No switching from on to off-hook | CPE front end damaged, for example due to lightning. |
| | Dial tone detection does not work | Voice transmission towards CPE broken.<br>CPE signal processor not working. |
| | No pulse digit detection | No standard pulse dialed. |

### 2.4.3.2 Universal Tone Detection (UTD) Test

The customer has to configure the UTD to detect the specified frequency and level. The UTD detects the start and end of the tone coming from the PCM interface (RX-IN point, see **Figure 30**) or from the analog line (TX-OUT point). The pass criteria and test outputs are described in detail in **Table 14**.

**Test Description**

- Configure the UTD with BBD coefficients
- Enable/Disable the UTD by calling the API function **DxsUtdEnable** or **DxsUtdDisable**.

**Table 14 Universal Tone Detection Pass Criteria and Test Outputs**

| | Test Details |
|---|---|
| Pass criteria | Pass/fail criteria have to be implemented in the customer's application layer, according to the customer's own specification. |
| Test output | The DXS UTD provides the start of the tone (UTD_START) and the end of the tone (UTD_END). |

**Table 15** describes how a given failure may be recognized from the universal tone detection test results.

**Table 15 Universal Tone Detection - Failure Causes**

| Test | Faulty Test Result | Possible Cause of Failure |
|---|---|---|
| | Tone start/end not detected | Voice transmission from the host towards the DXS broken. |

### 2.4.4 AC Level Meter

The DXS includes an integrated AC Level Meter that can be used to perform voice-band self tests in order to check the SLIC and codec functionality, or to verify the idle channel noise level in the channel under test. The AC Level Meter requires a known resistive termination between tip and ring (600 Ω), which can be switched in and out, see **Figure 30**.

**Test Description**

An integrated Digital Tone Generator (DTG) allows different types of AC measurements with a programmable frequency and level. The 8 kHz sampled AC test signal from the DTG flows through the standard voice DA path from the 8 kHz domain to the tip and ring wires. The tip-ring Test-In resistance loops the generated AC current back to the 8 kHz domain through the voice AD path. The DA and AD paths are the same signal paths as for the voice during a telephone call.

Different types of AC measurements can be performed to reproduce standard AC tests as offered by typical PCM measurement devices available on the market (see for example Q.552 **[22]**). The AC tests can be started from ACTIVE mode by calling the **DxsAcLmMeasurementStart** API. It is also permitted to call this API from DISABLED mode. In this case, the API internally sets ACTIVE mode before performing the AC measurements, and restores the original DISABLED mode at the end. An error is generated by this API if the initial mode is neither ACTIVE nor DISABLED.

The results are read out using the **DxsAcLmMeasResNumGet** API. A suitable BBD coefficient file for an impedance of 600 Ω has to be downloaded before running the AC tests.

### 2.4.4.1 AC Transhybrid Loss Test

The goal of this test is to verify the transhybrid filters of the codec, see **Figure 30**. The level of the DTG test signal is set to 0 dBm0. The frequency is swept from 100 Hz to 3700 Hz in 100 Hz steps. The transhybrid filters are enabled.

This function returns the absolute value of the AC signal at the TX-OUT point. For each frequency, the original amplitude of the test tone, 0 dBm0, is reduced by the transhybrid filters according to the following equation:

$$\text{Output(f) [dBm0]} = 0\ \text{dBm0} + \text{ThLoss(f)} \quad (6)$$

where the ThLoss(f) values are negative (signal attenuation) and in dB.

**Figure 35** shows the typical results of the AC transhybrid loss test and propose the masks for the implementation of the pass-fail criteria. The ThLoss results in this example were obtained by terminating the tip and ring wires with 600 Ω.

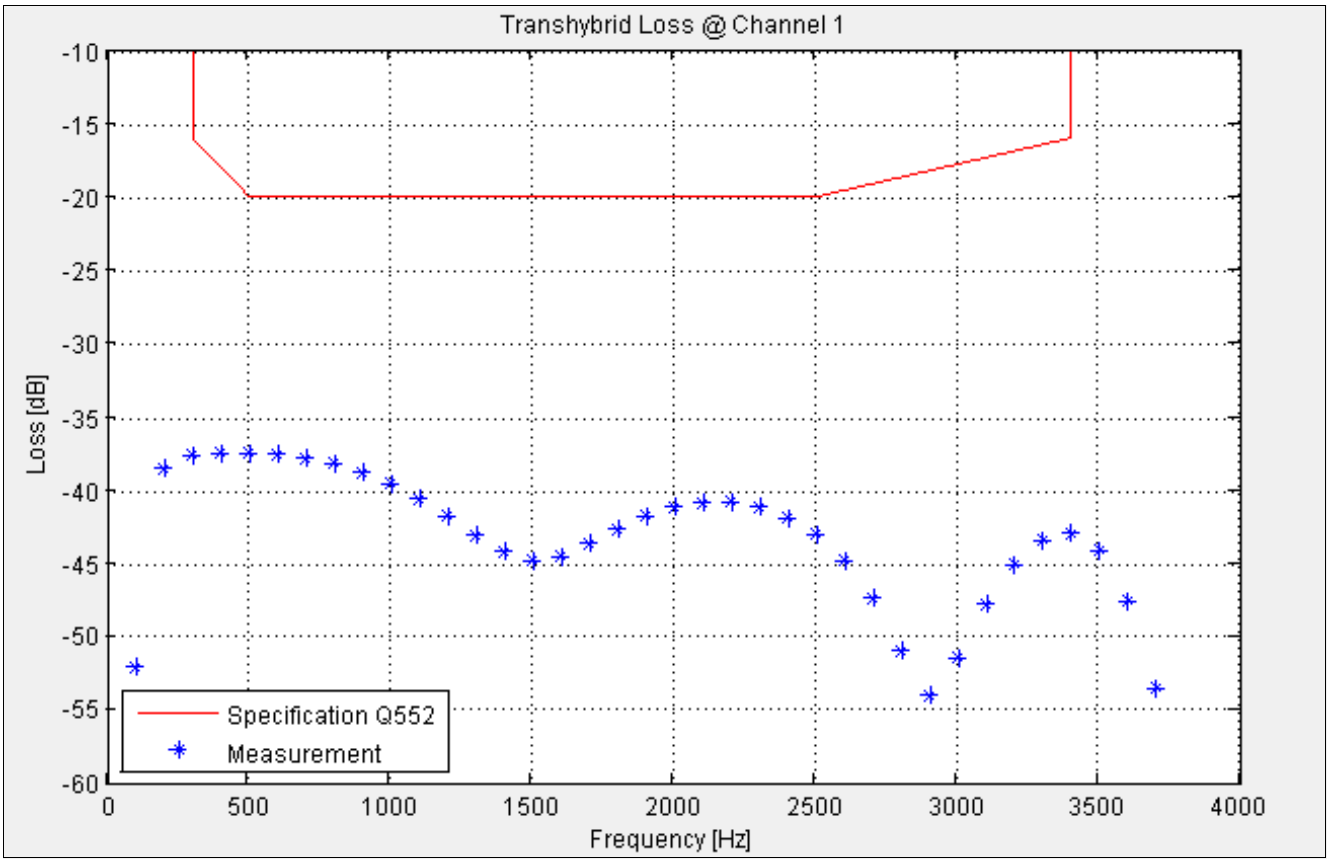


**Figure 35 Typical Results of AC Transhybrid Loss Test**

### 2.4.4.2 AC Frequency Response Test

The goal of this test is to measure the overall frequency response from the RX-IN point to the TX-OUT point, see **Figure 30**. The level of the test tone is set to -10 dBm0. The frequency is swept from 100 Hz to 3500 Hz in 100 Hz steps. The transhybrid filters are disabled. The resulting frequency response is relative to the AC level at 1000 Hz.

**Figure 36** shows the typical results of the AC frequency response test and propose the masks for the implementation of the pass-fail criteria. The results in this example were obtained by terminating the tip and ring wires with 600 Ω.

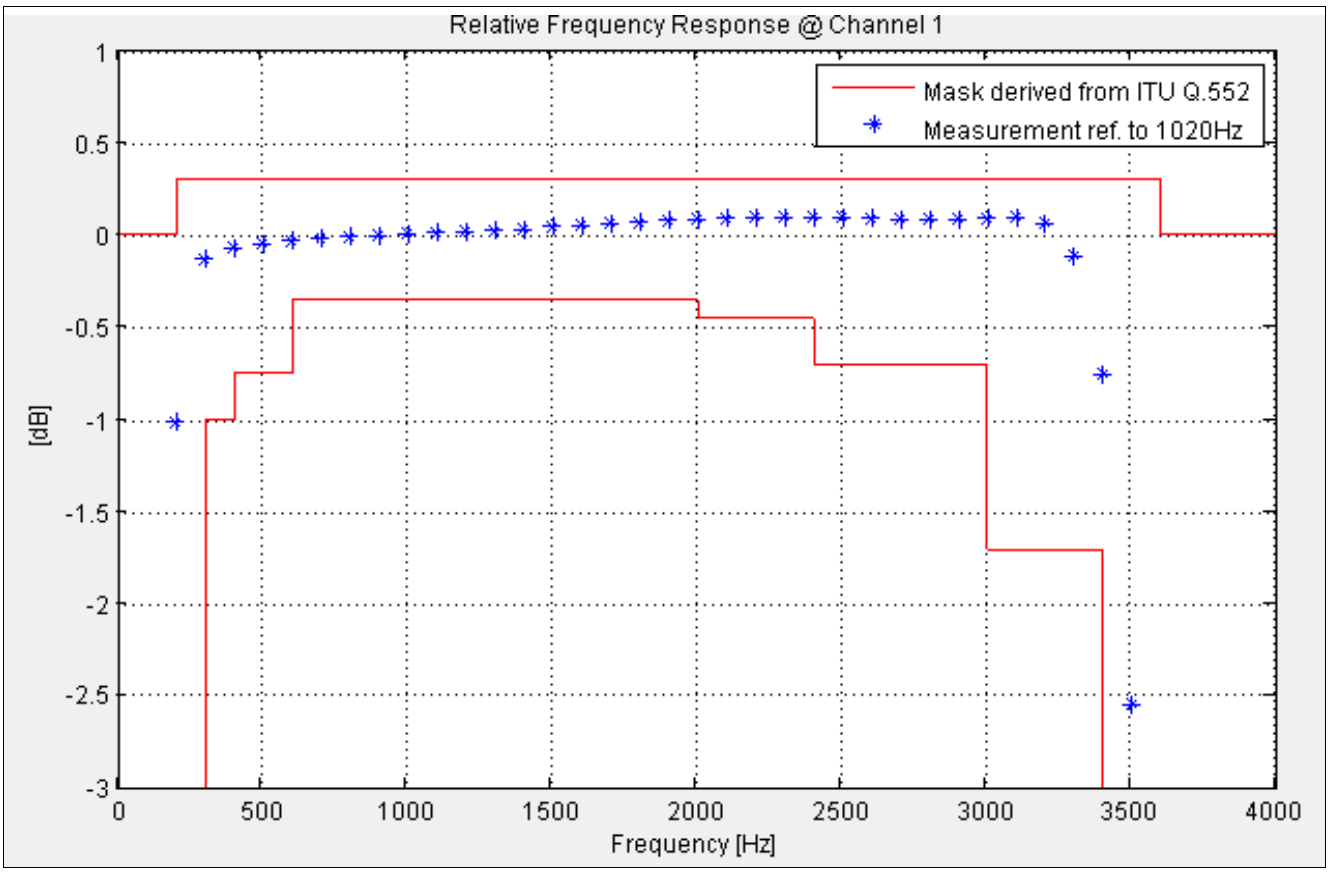


**Figure 36 Typical Results of AC Frequency Response Test**

### 2.4.4.3 AC Gain Tracking Test

The goal of this test is to measure the overall gain tracking of the AD and DA paths. The level output by the DTG is automatically increased from -59 dBm0 up to 3 dBm0 in 2 dB steps. The transhybrid filters are disabled. The frequency is set to 1020 Hz and the gain is measured relative to a reference value of -10 dBm0.

**Figure 37** shows the typical results of the AC gain tracking test and propose the masks for the implementation of the pass-fail criteria. The results in this example were obtained by terminating the tip and ring wires with 600 Ω.

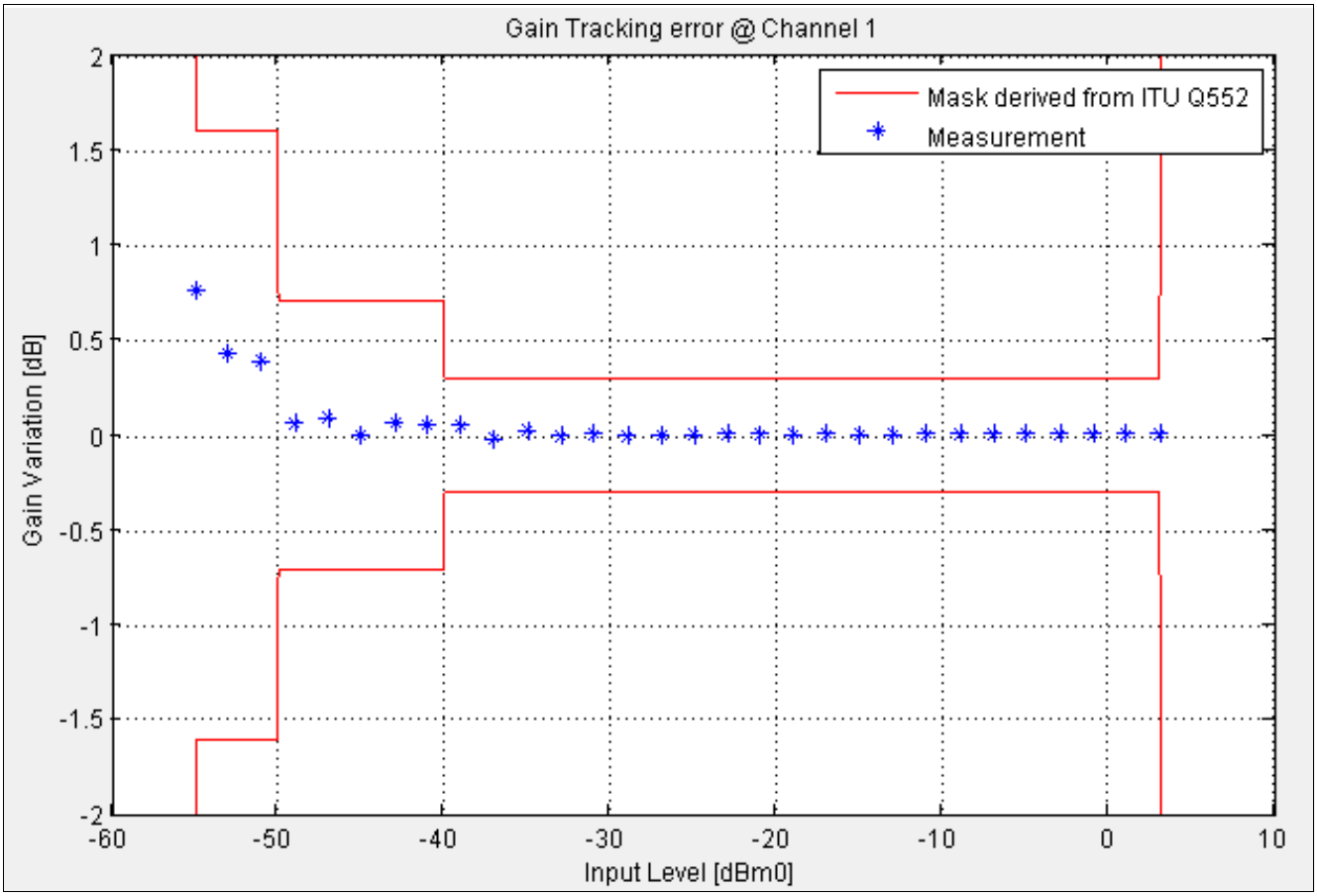


**Figure 37 Typical Results of AC Gain Tracking Test**

### 2.4.4.4 AC SNR Test

This test combines a level measurement with a total noise and distortion measurement. The test frequency is set to 1020 Hz. The test simultaneously measures the amplitude of a test tone at the TX-OUT point by means of selective bandpass filtering, and the total noise and distortion by means of a notch filter. Both the bandpass filter and notch filter are tuned to the test frequency 1020 Hz. The SNR is calculated as the difference between the outputs of the bandpass and notch filters. The transhybrid filters are disabled during this test.

**Figure 38** shows the typical results of the AC SNR test and propose the masks for the implementation of the pass-fail criteria. The results in this example were obtained by terminating the tip and ring wires with 600 Ω.

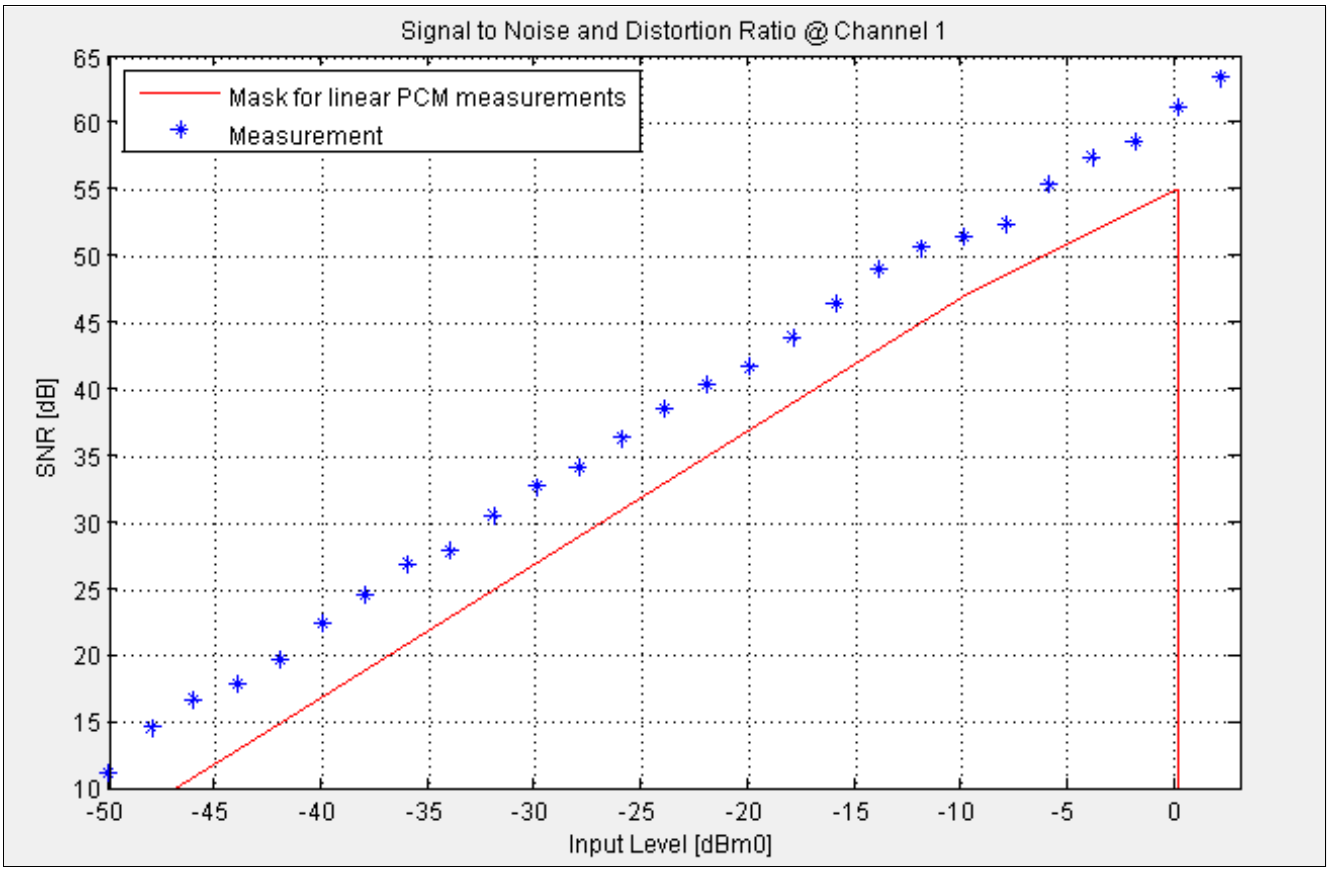


**Figure 38 Typical Results of AC SNR Test**

# 3 Device Driver and API Functions

## 3.1 DXS API Device Driver

The DXS API Device Driver is a User Space library that provides a set of APIs to access and control DXS features.

## 3.2 DXS Application Programming Interface (API)

The telephony, signaling and line testing functionality of the DXS is controlled using the DXS API (via the DXS API Device Driver). The API supports the following DXS features:

- POTS services (hook detection, line feeding, ringing, caller ID, metering, etc.)
- PCM interface control
- Tone generation and detection (DTMF, UTD, etc.)
- Line testing services (including GR-909 measurements, capacitance measurements and calibration)
- Event reporting services

A detailed description of the DXS API, including compilation, initialization, program interface descriptions and details about the function calls, can be found in **[5]**. The main API functions are listed in **Table 16**.

**Table 16 DXS API Functions**

| Function Call | Short Description |
|---|---|
| **Initialization** | |
| DxsInit | API Driver initialization, DXS device access setup |
| DxsExit | API Driver deinitialization, DXS device access wrap-up |
| DxsPatch | DXS PRAM patch download |
| DxsBBD | DXS BBD download |
| DxsCapabilitiesRead | DXS firmware capabilities read |
| DxsVersionRead | DXS version read |
| DxsSleepEnable | Sleep condition enable |
| DxsSleepDisable | Sleep condition disable |
| **Configuration** | |
| DxsPcmInterfaceEnable | PCM interface configuration and enable |
| DxsPcmChannelEnable | PCM channel configuration and enable |
| DxsPcmChannelDisable | PCM channel deactivation |
| DxsPcmChannelMute | PCM channel mute in RX direction |
| DxsPcmChannelUnmute | PCM channel unmute in RX direction |
| DxsRingConfig | Configure ringing parameters |
| DxsMwIConfig | Configure message waiting lamp parameters |
| DxsGainsSet | Digital gain configuration |
| DxsGainsGet | Digital gain value retrieval |
| **Control** | |
| DxsLineModeSet | Set new line mode |
| DxsLineModeGet | Read current line mode |
| DxsClockFailLineFeedFreeze | Disable automatic switching to ESD in case of clock fail |

**Table 16 DXS API Functions** (cont'd)

| Function Call | Short Description |
|---|---|
| DxsClockFailLineFeedUnFreeze | Restore automatic switching to ESD in case of clock fail |
| **Tone Generation** | |
| DxsToneConfig | Configure Tone Generator |
| DxsToneEnable | Tone Generator enable |
| DxsToneDisable | Tone Generator disable |
| **FSK Caller ID Generation** | |
| DxsFskConfig | Configure FSK Generator |
| DxsFskEnable | FSK Generator enable |
| DxsFskDisable | FSK Generator disable |
| DxsFskData | Provide new data buffer for FSK Generator |
| DxsCidInit | Initialize CID interface |
| DxsCidTimerConfig | Configure CID timers |
| DxsCidMsgSetup | Create or update the CID message per channel |
| DxsCidMsgReset | Clean message configuration entirely per channel |
| DxsCidTypeIMsgStart | Start CID Type I sequence playout |
| DxsCidTypeIIMsgStart | Start CID Type II sequence playout |
| DxsCidSeqStop | Stop CID sequence playout |
| **Tone Detection** | |
| DxsUtdEnable | Universal Tone Detector enable |
| DxsUtdDisable | Universal Tone Detector disable |
| **DTMF Detection** | |
| DxsDtmfConfig | Configure DTMF Detector |
| DxsDtmfEnable | DTMF Detector enable |
| DxsDtmfDisable | DTMF Detector disable |
| **Pulse Dialing Detection** | |
| DxsHookValTimeSet | Configure validation time intervals for hook state machine |
| **Metering** | |
| DxsMeteringPulseEnable | Enable Metering (TTX) pulse |
| DxsMeteringPulseDisable | Stop Metering (TTX) pulse |
| **Continuous Measurement** | |
| DxsContMeasurementResultGet | Read continuous measurement results |
| **GR-909 Measurement** | |
| DxsGR909LimitsSet | Program limit values for GR-909 tests |
| DxsGR909LimitsGet | Read current limit values for GR-909 tests |
| DxsGR909ResultGet | Read GR-909 test results |
| **Analog Line Calibration** | |
| DxsCalibrationGet | Read analog line calibration results |
| DxsCalibrationSet | Set analog line calibration values |

**Table 16 DXS API Functions** (cont'd)

| Function Call | Short Description |
|---|---|
| **Open Loop Calibration for Line Testing** | |
| DxsOpenLoopCalibration | Perform open loop calibration for GR-909 and capacitance tests |
| DxsOpenLoopConfigSet | Configure open loop calibration values |
| DxsOpenLoopConfigGet | Read open loop calibration results |
| **Capacitance Measurement** | |
| DxsCapMeasurementResultGet | Read latest capacitance measurement results |
| **AC Level Meter Measurement** | |
| DxsAcLmMeasurementStart | Start AC Level Meter (ACLM) measurement |
| DxsAcLmMeasResNumGet | Get the number of available ACLM measurement results |
| DxsAcLmMeasResArgGet | Get the argument of a measurement point |
| DxsAcLmMeasResValGet | Get the value of a measurement point |
| **GPIO Pin Control Interface** | |
| DxsGpioPortConfig | Configure GPIO lines |
| DxsGpioWrite | Set the GPIO line output value |
| DxsGpioRead | Read the GPIO line input value |
| **Event Reporting** | |
| DxsWaitListInit | Initialize waiting list |
| DxsWaitListDestroy | Deinitialize waiting list |
| DxsWaitListDevAdd | Add a device to waiting list |
| DxsWaitListDevRemove | Remove a device from waiting list |
| DxsWaitForEvent | Wait for events |
| DxsEventGet | Read a single event from the device |

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***Attention: Please refer to the latest revision of these documents.***

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