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MaxLinear

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
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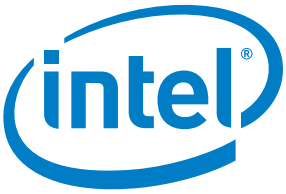

Intel® SLIC for CPE

SLC210 (PEF41078VV11)

Data Sheet

Revision 2.0, 2017-09-05
Intel Confidential
Reference ID 617968

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Revision History

Current:	**Revision 2.0, 2017-09-05**
Previous:	**Revision 1.0, 2015-11-23**
Page	**Major changes since previous revision**
All	The products described in this document have been rebranded with new ordering codes and names: • "SLIC 200", "Smart Subscriber Line Interface Circuit" renamed "Intel® SLIC for CPE" • SLIC 210 renamed SLC210
9	**Table 1 Product and Package Naming** updated.
13	**Table 4 Power Pins**: Description of GNDC pin updated - can optionally be connected to GND.
43	**Literature References** updated.

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Preface

This Data Sheet describes the hardware features of the SLC210 (PEF41078VV11) device, an Intel® SLIC for CPE product.

To simplify matters, the following synonyms are used:

SLIC

Synonym used for the SLC210 (PEF41078VV11) device.

Voice Controller

Synonym used for a device using the Intel POTS control firmware and voice DSP functionality, with the ability to connect to the SLC210 via the Intel SSI interface.

Organization of this Document

This document is organized as follows:

- **Chapter 1**, **General Description / Introduction**
  A general description of the chip set, key features/requirements and typical applications.
- **Chapter 2**, **Pin Configuration for SLC210**
  Pin diagram and pin description.
- **Chapter 3**, **DC/DC Converter Hardware**
  Support of DC/DC converter hardware.
- **Chapter 4**, **Functional Description**
  Operating modes, hardware behavior and handling.
- **Chapter 5**, **Interfaces**
  SSI Interface.
- **Chapter 6**, **Typical Application Circuit**
  Reference schematics and external components for typical applications.
- **Chapter 7**, **Electrical and Transmission Characteristics**
  Operating conditions and characteristics, limit values.
- **Chapter 8**, **Hardware Design Guidelines**
  Layout recommendations and design guidelines for board design.
- **Chapter 9**, **Package Outline**
  Illustrations and dimensions of the package outline.
- **Literature References** and **Standards References**
  List of referenced documents and standards.
- **Terminology**
  List of abbreviations.

1 General Description / Introduction

The SLC210 implements a single channel telephone line interface (FXS) in a single package optimized for Customer Premises Equipment (CPE) applications and Small and Medium-sized Enterprise (SME) applications.

The high voltage part of SLC210 is able to provide differential output voltages of up to 144 Vp. In all modes of operation an optimized battery supply voltage is generated by means of a DC/DC converter controlled by an integrated PWM controller. The SLC210 is connected to specific voice controllers via the proprietary Smart SLIC Interface (SSI).

All the relevant parameters can easily be programmed via software, thus allowing the requirements of all regions in the world to be met with a single hardware design.

1.1 Features

- Single channel line interface (FXS) with integrated ringing
- Integrated 1.5 V regulator (see **Section 1.2**)
- DC/DC based generation of optimized negative supply voltage
- Minimum power dissipation in all operating modes (patented solution for ringing)
- DC feeding up to 50 mA
- Optimized for accurate line testing
- Low cost Bill of Materials (BoM)
- Enables high density system solutions
- SLC210 packaged in PG-VQFN-48

Table 1 Product and Package Naming

Product Name	Former Lantiq Sales Code	Ordering Code	S-Spec#	Package
SLC210	PEF 41078 V V1.1	PEF41078VV11	SLLFZ	PG-VQFN-48

1.2 Integrated 1.5 V Regulator

The SLC210 is either operated using an external 1.5 V supply, or by taking advantage of its integrated 1.5 V regulator in the case of systems where a 1.5 V supply is not available. If an external 1.5 V supply is to be used, the REG_MODE pin should be left open, allowing the device to be supplied from this external 1.5 V source.

If the integrated 1.5 V regulator is used, it can be run in either linear mode or step-down (buck) mode depending on the requirements as follows.

- For lowest cost applications, select linear mode by connecting the REG_MODE pin to GND. Add one small 1.5 Ω resistor between REG_OUT and VDD15. The regulator operates as an LDO.
- If lowest power dissipation is desired, connect the REG_MODE pin to VDD3V3 and place a small coil of approx. 3.3 µH between REG_OUT and VDD15. The regulator operates in step-down mode with an efficiency of approx. 80%.

1.3 Logic Symbol

Figure 1 shows the logic diagram for the SLC210.

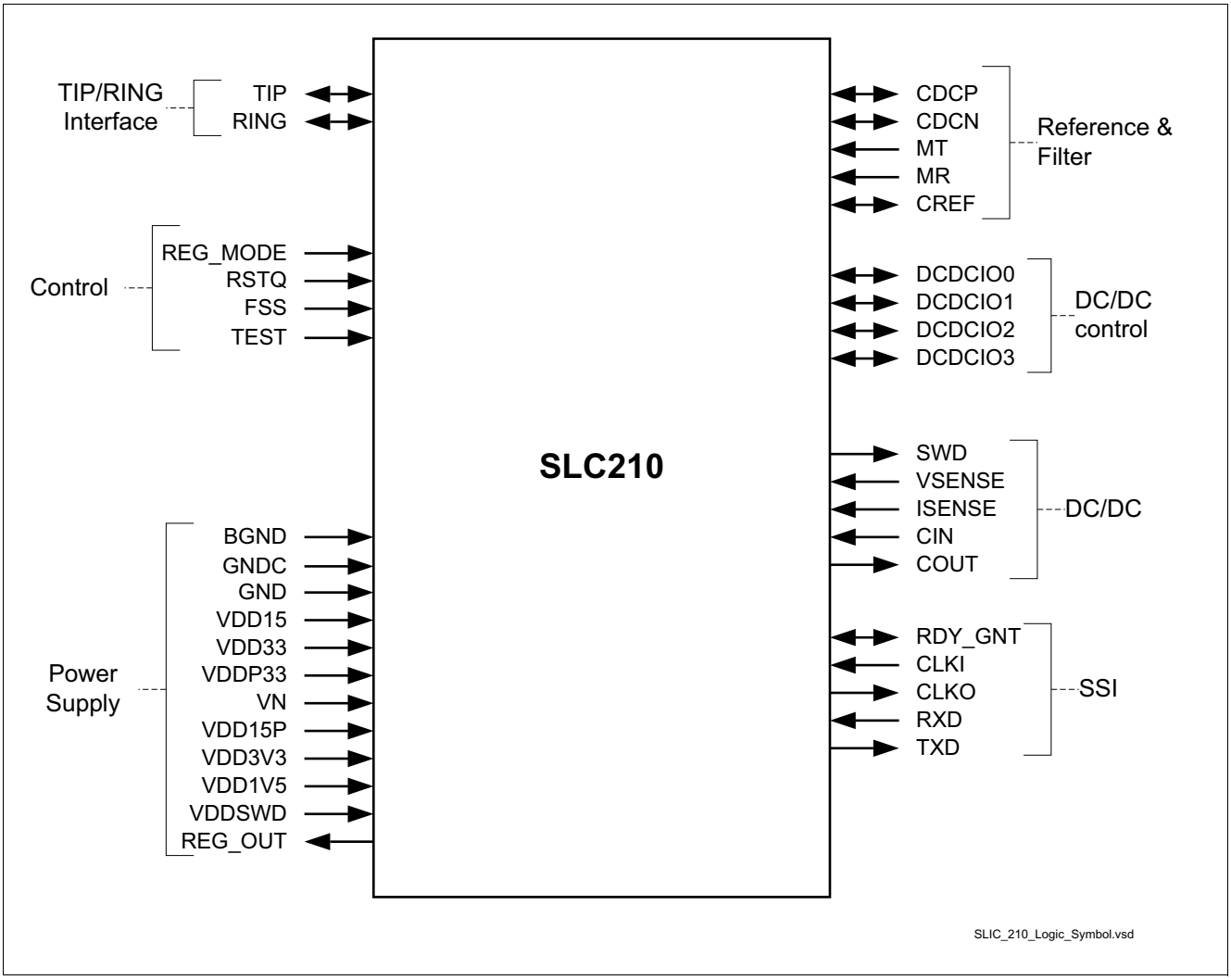


Figure 1 Logic Symbol for SLC210

1.4 Block Diagram

Figure 2 shows the block diagram for the SLC210.

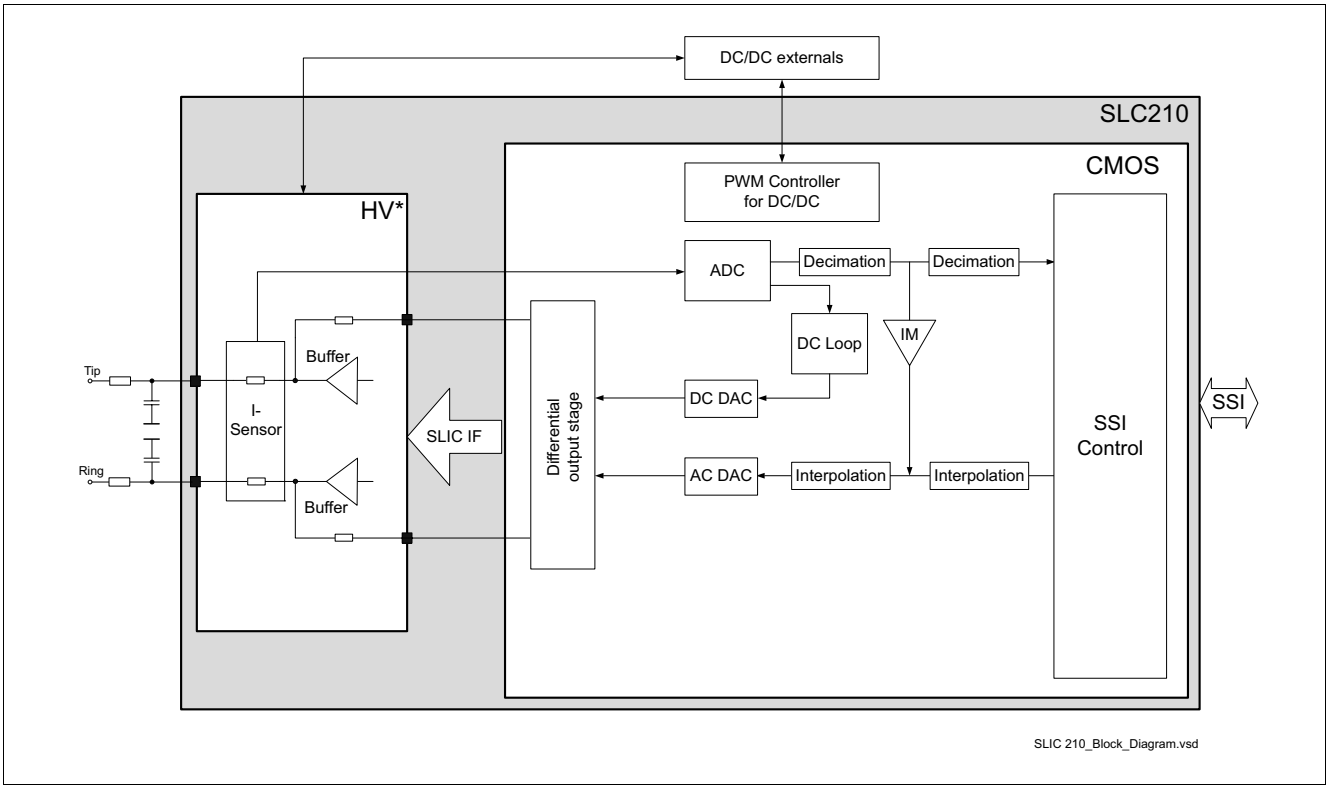


Figure 2 SLC210 Block Diagram

The SLC210 is a complete single channel line interface consisting of one high-voltage SLIC with integrated ringing and a CMOS mixed signal chip. The SLC210 also includes a PWM controller for the DC/DC converter. This generates the optimum battery supply voltage to minimize power dissipation (see **Chapter 6** for further details).

The system is based on a voltage feed / current sense concept with programmable control loops for all the relevant AC and DC parameters to ensure the highest flexibility.

2 Pin Configuration for SLC210

2.1 Pin Diagram

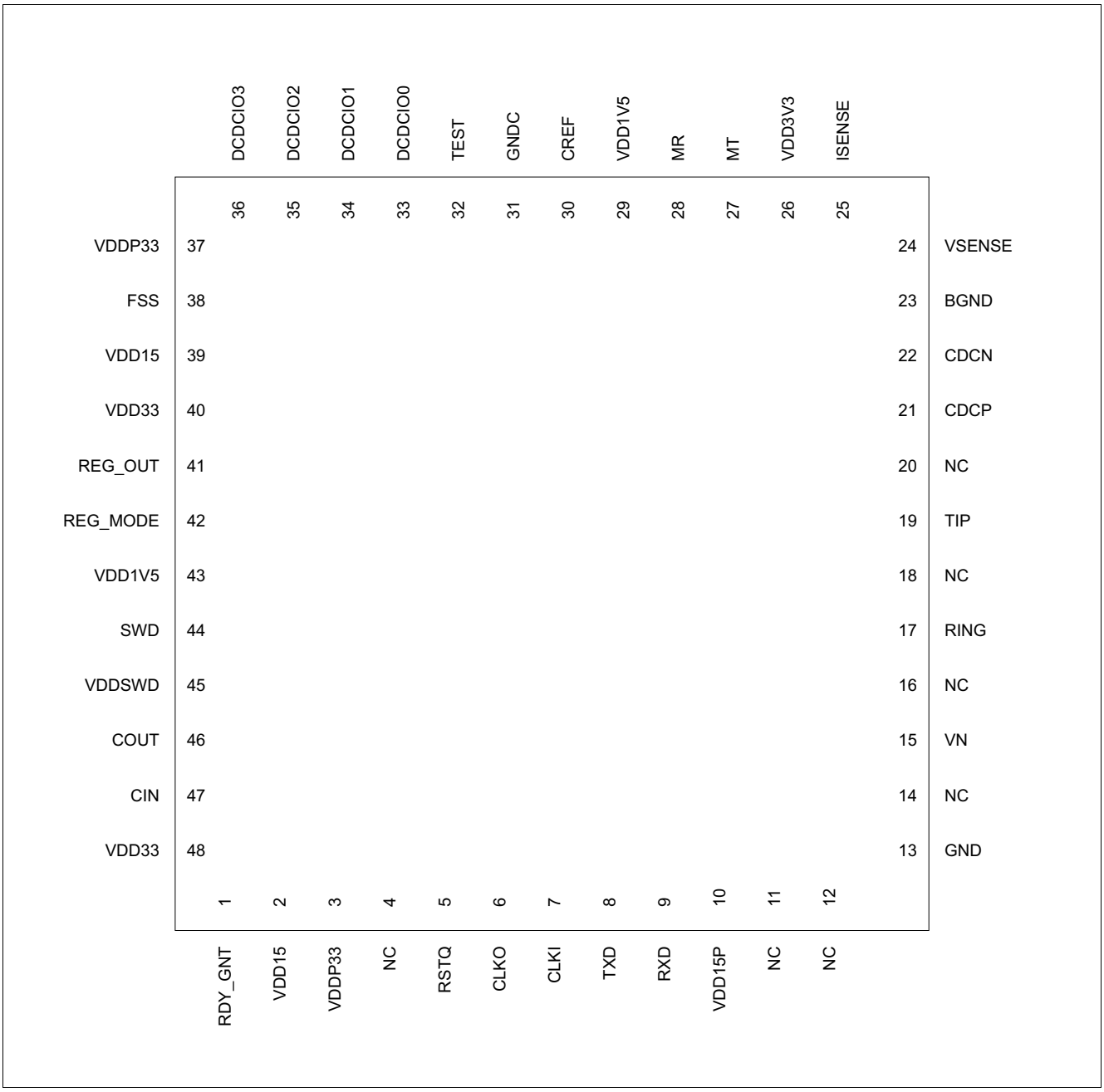


Figure 3 Pin Configuration PG-VQFN-48 Package (Top View)

2.2 Pins Sorted by Function

Table 2 Abbreviations for Pin Type

Abbreviations	Description
I	Input. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal. Digital levels.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	I/O is a bidirectional input/output signal. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 3 Abbreviations for Buffer Type

Abbreviations	Description
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.

2.2.1 Power and Ground Pins

Table 4 Power Pins

Pin No.	Name	Pin Type	Buffer Type	Function
29, 43	VDD1V5	PWR	–	**+1.5 V Analog Supply Voltage**
10	VDD15P	PWR	–	**+1.5 V PLL Supply Voltage**
26	VDD3V3	PWR	–	**+3.3 V Analog Supply Voltage**
40, 48	VDD33	PWR	–	**+3.3 V Digital Supply Voltage**
2, 39	VDD15	PWR	–	**+1.5 V Digital Supply Voltage**
45	VDDSWD	PWR	–	**Positive Supply for SWD Pins/Charge Pump Output**
3, 37	VDDP33	PWR	–	**Digital Pad Supply Voltage** Typically 3.3 V, but 2.5 V or 1.8 V can also be used.
41	REG_OUT	PWR	–	**Output of +1.5 V Regulator**
15	VN	PWR	–	**DC/DC Converter Output** Regulated negative SLIC battery voltage (V_N > -150 V)
13	GND	GND	–	**Ground**

Table 4 Power Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
31	GNDC	GND	–	**Ground for CREF** Can be optionally connected to GND.
23	BGND	GND	–	**Battery Ground**

2.2.2 Control Pins

Table 5 Reference and Reset Pins

Pin No.	Name	Pin Type	Buffer Type	Function
5	RSTQ	I	–	**Chip Reset** Active low
30	CREF	AI/O	–	**External Filter Capacitor**
42	REG_MODE	I	–	**1.5 V Supply Select**
38	FSS	PWR	–	**Production Test** Must be connected to GND
32	TEST	I	–	**Production Test** Must be connected to GND

2.2.3 SSI Interface Pins

Table 6 SSI Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
1	RDY_GNT	I/O	PP	**Serial Interface Ready/Grant** Do not use, do not connect.
7	CLKI	I	–	**Clock In (Master Clock)**
6	CLKO	O	PP	**Serial Interface Clock Out**
9	RXD	I	–	**Serial Interface Receive**
8	TXD	O	OD/PP	**Serial Interface Transmit**

2.2.4 Analog Signal Pins

Table 7 Analog Signal Pins

Pin No.	Name	Pin Type	Buffer Type	Function
21	CDCP	AI/O	–	**DC Voltage Filter** External capacitance for DC voltage filtering
22	CDCN	AI/O	–	**DC Voltage Filter** External capacitance for DC voltage filtering
27	MT	AI	–	**Measurement, Tip** Input for measurement and testing from tip
28	MR	AI	–	**Measurement, Ring** Input for measurement and testing from ring

2.2.5 Subscriber Line Interface Pins

Table 8 Subscriber Line Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
19	TIP	AI/O	–	**Tip** Subscriber loop connection, tip
17	RING	AI/O	–	**Ring** Subscriber loop connection, ring

2.2.6 DC/DC Control Pins

Table 9 DC/DC Control Pins

Pin No.	Name	Pin Type	Buffer Type	Function
25	ISENSE	AI	–	**Current Sense Input** Sense pin for limitation of switch transistor current
24	VSENSE	AI	–	**Voltage Sense Input** Sense pin for DC/DC converter output voltage
44	SWD	O	PP	**Switching Driver Output** Switching transistor driver output
46	COUT	AO	–	**Connection for Charge Pump Capacitor**
47	CIN	AI	–	**Connection for Charge Pump Capacitor**

2.2.7 DC/DC Hardware Control Pins

The DC/DC converter type is coded via the DC/DC hardware control pins. For further details refer to **Chapter 3**.

Table 10 DC/DC Hardware Control Pins

Pin No.	Name	Pin Type	Buffer Type	Function
33	DCDCIO0	I/O	PP	**Reserved for DC/DC Control** Internal pull-up resistors, which are activated by the internal firmware, are connected to these pins.
34	DCDCIO1	I/O	PP	
35	DCDCIO2	I/O	PP	
36	DCDCIO3	I/O	PP	

2.2.8 Not Usable Pins

Table 11 Not Usable Pins

Pin No.	Name	Pin Type	Buffer Type	Function
4, 11, 12, 14, 16, 18, 20	NC	NC	–	**Do not connect**

3 DC/DC Converter Hardware

The DC/DC converter hardware type and usage is coded via the DCDCHW pins as described in **Table 12**.

Attention: Not all of the DC/DC converters described in Table 12 are supported by current system packages. Please refer to product specific system release information for further details on individual DC/DC converter types.

Table 12 Coding for DC/DC Converter Hardware Type

DC/DC Converter Type	Coding Pin Connections			
	DCDCIO3	DCDCIO2	DCDCIO1	DCDCIO0
Inverting buck-boost converter Combined inverting buck-boost converter	open	open	Control of test load switch channel B	Control of test load switch channel A
Inverting flyback converter Combined inverting flyback converter Inverting boost converter	GND	open	Control of test load switch channel B	Control of test load switch channel A
Buck-or-boost converter Combined buck-or-boost converter	STANDBY hook detector channel B	STANDBY hook detector channel A	Inverted SWD output for channel B	Inverted SWD output for channel A

4 Functional Description

4.1 Operating Modes

The SLC210 operates in the following modes, controlled by the voice controller via the SSI.

Table 13 System State Description[1)]

System State	Description
DISABLED	The SLC210 is disconnected from the phone line. DC/DC converter is switched off.
STANDBY	Off-hook detection possible, no AC transmission.
ACTIVE	Voice transmission and on/off-hook detection as well as line monitoring possible. DC line feeding with programmed DC characteristic.
RING_BURST	Generation of high-voltage ring signal using patented supply voltage tracking concept.

1) Additional modes, such as line testing, calibration and ground start, may be available depending on the voice controller firmware.

4.2 Hardware Behavior and Handling

4.2.1 Reset

Hardware Reset

The frequency detection block starts when the RSTQ pin is released. The CLKI input frequency must be n * 512 kHz (where n is 1, 2, 3, 4, 5, 6, 7, 8, 16). An internal boot process that is part of the control logic configures the SSI interface. Once communication has been established, the SLC210 is configured within 3 ms of RSTQ being released.

Software Reset

A reset can also be initiated by a software command via the SSI interface. The boot process after reset is the same as for a hardware reset, except that the frequency detection is not performed.

Out of Sync Reset / Clock Fail Reset

An out of sync reset will be triggered if the frame-sync symbol, which is transmitted over the SSI interface, is not received within a predefined period of time. A clock fail reset will be triggered if a frame does not consist of exactly 256 symbols. The process follows the same steps as a software reset.

5 Interfaces

5.1 SSI - Smart SLIC Interface

The Smart SLIC Interface (SSI) module is a bidirectional interface for voice and control data, designed to reduce the number of connections required between the SLC210 and any device connected to it.

Figure 4 shows the connections to the SLC210.

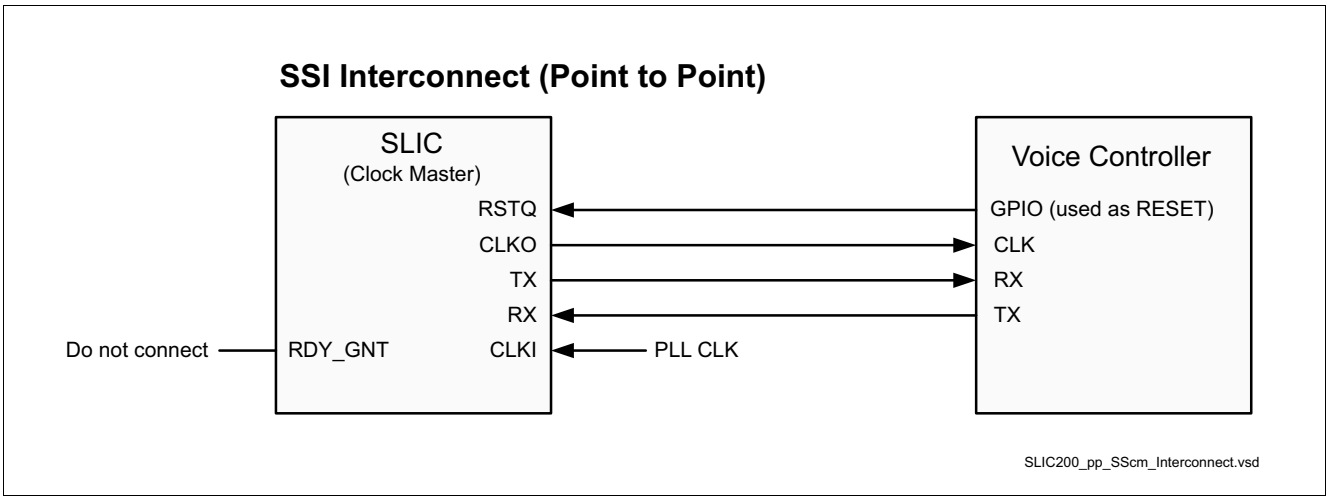


Figure 4 Connections to SLC210

5.1.1 SSI Timing Diagram

Figure 5 together with **Table 14** illustrates the relationship between the clock signals and the data paths.

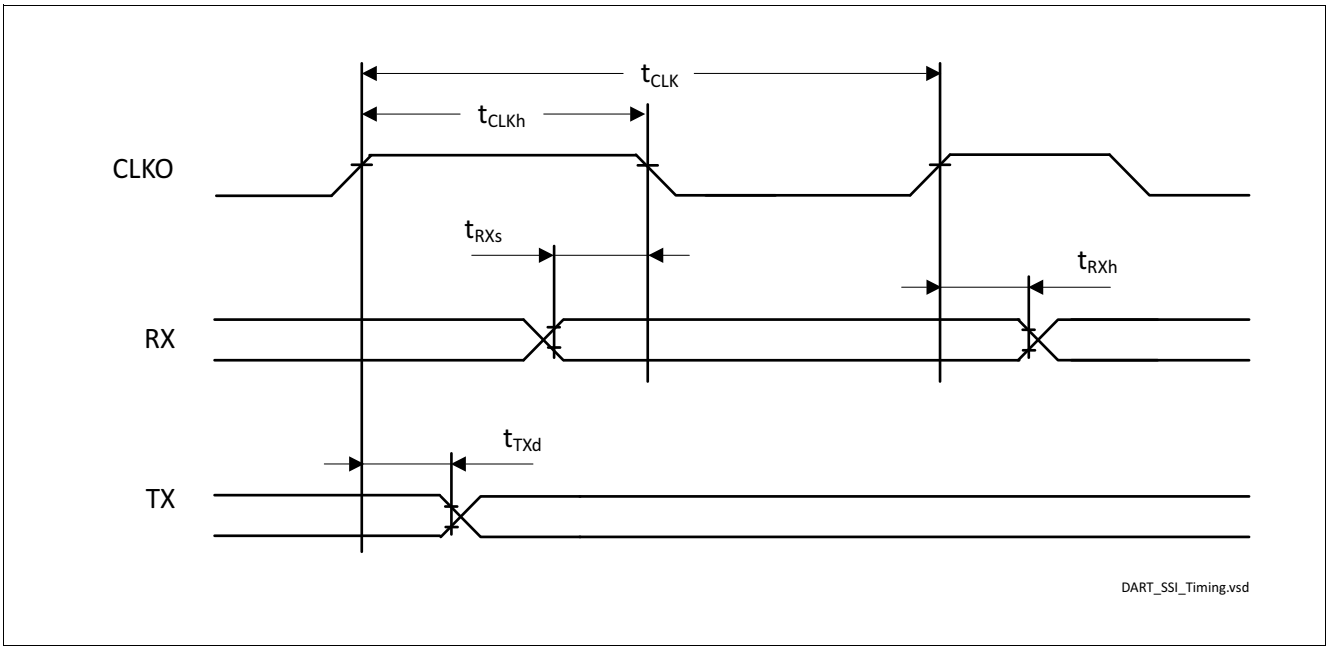


Figure 5 SSI Timing

Attention: Within an SSI transmission frame, the position of bits in both receive (RX) and transmit (TX) data streams is well-defined. Any delay in the TX or RX paths must be kept short enough to ensure that the RX and TX bit positions do not become out-of-sync, that is neither RX nor TX data may be delayed into the next clock cycle, otherwise the SLC210 will reset.

Table 14 SSI Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CLKO period	t_{CLK}	–	30.5176	–	ns	–
CLKO duty cycle	t_{CLKh}	–	50	–	%	–
RX setup	t_{RXs}	2	–	–	ns	–
RX hold	t_{RXh}	2	–	–	ns	–
TX delay	t_{TXd}	4	–	10	ns	30 pF capacitive load

5.1.2 External Clock Drive at CLKI

Figure 6 shows the timing and **Table 15** the appropriate timing parameter values required on the CLKI pin.

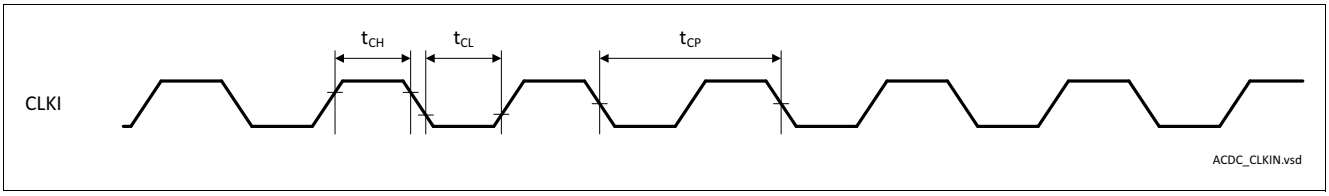


Figure 6 External Clock Drive CLKI

Table 15 External Clock Drive CLKI

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock frequency	$1/t_{CP}$	–	n * 512	–	kHz	n = [1,2,4,8]
CLKI jitter phase noise density, 1 kHz frequency offset	–	–	–	-80	dBc[1)]/Hz	–
CLKI long term jitter	–	–	–	0.5	ns_{RMS}	–

1) dBc = dB carrier.

6 Typical Application Circuit

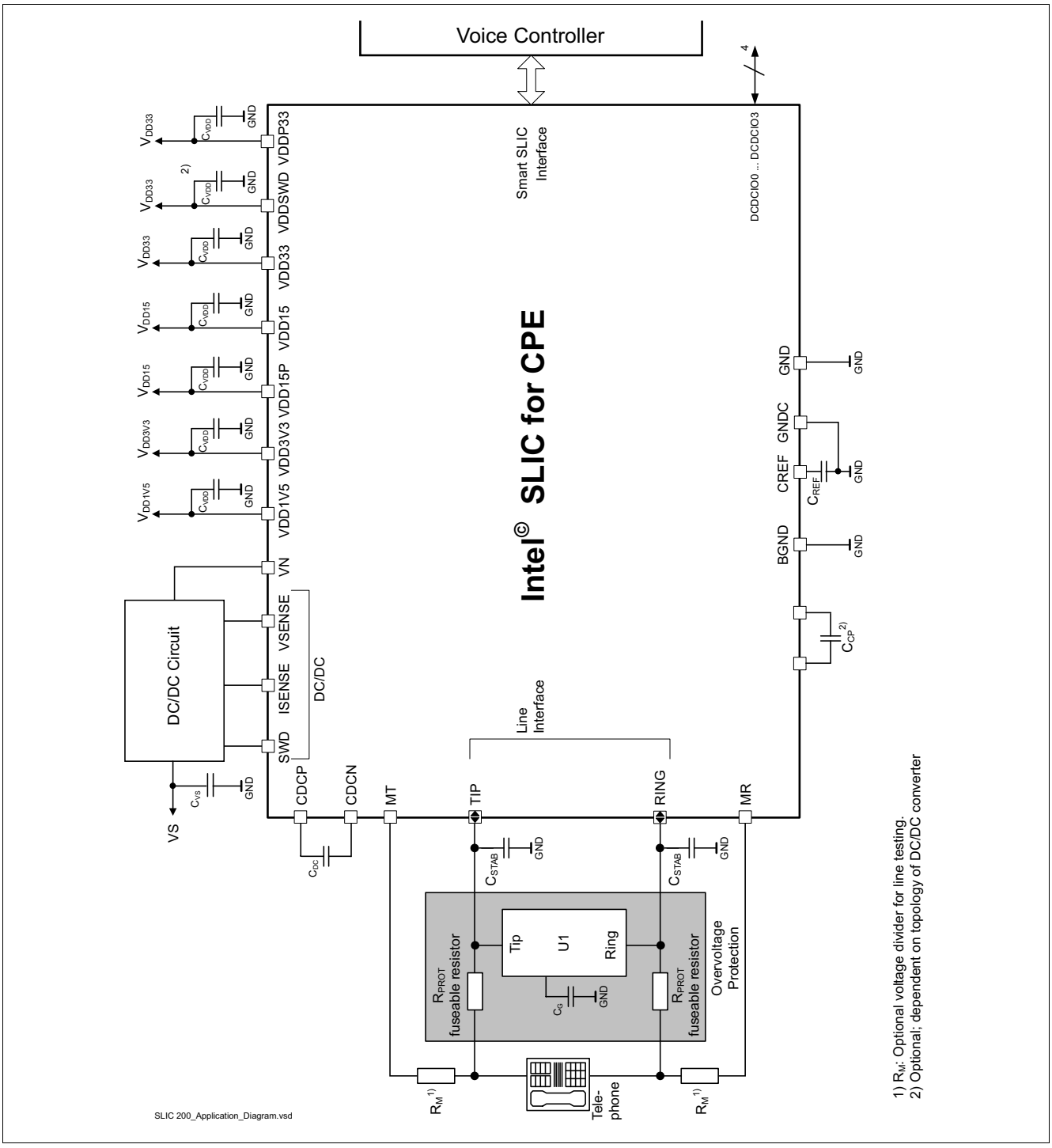
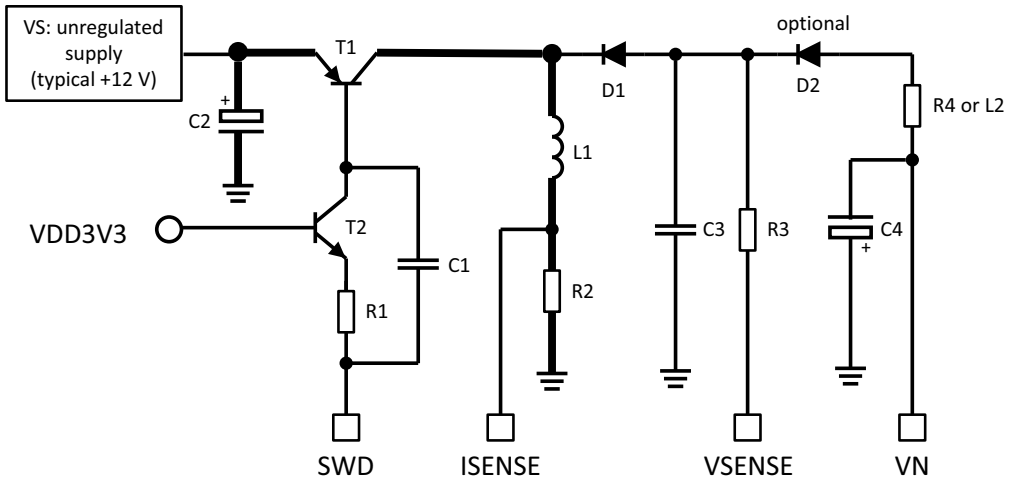


Figure 7 Application Circuit for FXS Operation

The circuit shown in **Figure 7** is equipped with a DC/DC converter based on a pnp transistor switch, as shown in **Figure 8**. This is the recommended default circuit.

The application circuit in **Figure 7** can be equipped with a DC/DC converter as described in the example DC/DC converter circuit presented in this chapter:

- **Inverting buck-boost DC/DC converter with input voltage +12 V (IBB12)**, see **Figure 8**
  A standard application with a dedicated DC/DC converter. This is the recommended default circuit.



Component D2 only has to be used when the gate triggered negative polarity protector for ITU-T K.21 basic requirements is used (refer to the protection requirements application note).

For improved ripple rejection or if diode D2 is used, replace resistor R4 with inductor L2.

DXS_DCDC_converter_bipolar_dedicated.vsd

Figure 8 Inverting Buck-Boost Converter Circuit for 12 V (IBB12)

6.1 Bill of Materials

Table 16 shows the external passive components required for a single channel solution with protection as shown in the figures above. The supply input is 12 V and the ringing voltage is 65 V_{RMS} with no DC offset for ringer loads of up to 3 REN or up to 5 REN with ring current regulation.

Depending on the ringing voltages used in the application, some of the device ratings may be reduced (see footnote [1] below Table 16).

Table 16 External Components in Application Circuit

Quantity	Symbol	Component Type	Value	Unit	Tolerance	Rating / Comments
SLC210 External Components incl. Protection, see Figure 7						
2	C_{STAB}	Capacitor	15	nF	10%	150 V[1]
2	R_M[2]	Resistor	1.5	MΩ	1%	0.25 W, 200 V[3]
1	C_{DC}	Capacitor	330	nF	10%	10 V
2	R_{PROT}	Resistor	36	Ω	1%	0.25 W (depending on protection requirements, refer to [3].
1	C_{REF}	Capacitor	220	nF	10%	10 V
1	*U1*	Protection element	–	–	–	Overvoltage protection, e.g. Bourns TISP 61089, refer to [3].
1	C_G	Capacitor	100	nF	20%	150 V[1], capacitor on gate of protection thyristor (refer to data sheet of protection element used)
7	C_{VDD}	Capacitor	Typ. 10[4]	µF	20%	10 V
Inverting Buck-Boost Converter Circuit T0.2 for 12 V, see Figure 8						
1	*C1*	Capacitor	47	nF	10%	10 V
1	*C2*	Capacitor	22	µF	20%	16 V, electrolytic type (low ESR)
1	*C3*	Capacitor	220	nF	10%	150 V[1], ceramic capacitor
1	*C4*	Capacitor	2.2	µF	10%	160 V[1], ECA2CM2R2 from Panasonic (electrolytic capacitor)
1	*D1*	Diode	–	–	–	150 V, 1 A, needs to be of “fast” or “ultra-fast” type, e.g. ES1C, MURS120 or equivalent
1	*L1*	Inductor	47	µH	20%	I_{PEAK} = 1.55 A, e.g. EPCOS B82464G4473
1	*R1*	Resistor	160	Ω	5%	0.1 W
1	*R2*	Resistor	82	mΩ	5%	0.25 W
1	*R3*	Resistor	1	MΩ	1%	150 V, 0.125 W
1	*R4*[5]	Resistor	20	Ω	5%	0.25 W
	L2	Inductor	220	µH	10%	0.1 A, TDK NLCV32T-221K-PF
1 optional	*D2*	Diode	–	–	–	200 V, 0.2 A, BAS21 or equivalent; optional, depending on used protection

Table 16 External Components in Application Circuit (cont'd)

Quantity	Symbol	Component Type	Value	Unit	Tolerance	Rating / Comments
1	*T1*	Transistor	–	–	–	Zetex DXT2014P5, PNP switching transistor; an alternative type is NXP PBHV9215Z (about 3% less efficiency)
1	*T2*	Transistor	–	–	–	SMBT3904S, NPN silicon transistor or equivalent

1) Depending on the maximum required voltage; for 65 V_{RMS} ringing, a device rating of 100 V is sufficient.
2) Voltage divider for line testing.
3) Depending on the protection requirements, resistor R_M may need to be split into more than one component (refer to **Chapter 8.2.2**).
4) Depends on layout considerations and the application (the sum of the capacitance of all C_{VDD} capacitors per voltage rail on the PCB should be of about 10 µF).
5) For improved ripple rejection or if diode *D2* is used, replace resistor *R4* with inductor *L2*.

7 Electrical and Transmission Characteristics

7.1 Absolute Maximum Ratings

Table 17 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltages at VDD15, VDD1V5, VDD15P referred to GND	–	-0.3	–	1.65	V	–
Supply voltages at VDD33, VDD3V3 referred to GND	–	-0.3	–	3.63	V	–
Ground voltage differences between GND, BGND, GNDC	–	-0.3	–	0.3	V	–
Supply voltage differences between VDD15, VDD1V5, VDD15P	–	-0.3	–	0.3	V	–
Analog test, filter and gain voltages	–	-0.3	–	3.63	V	V_{DD3V3} = 3.3 V, V_{DD1V5} = 1.5 V, V_{GND} = 0 V
Digital input and output voltages	–	-0.3	–	3.63	V	V_{DD33} = 3.3 V, V_{DD15} = 1.5 V, V_{GND} = 0 V
Digital input leakage current per pin	I_L	-50	–	50	µA	$0 \le V_{in} \le V_{DD33}$
DC input or output current at any input or output pin	–	–	–	100	mA	latch-up free
Storage temperature	T_{STG}	-55	–	125	°C	–
Total supply voltage	V_{DD3V3} - V_N	–	–	154	V	–
ESD Robustness						
ESD voltage (HBM)[1)]	–	–	–	2	kV	–
ESD voltage (CDM)[2)]	–	–	–	1	kV	–

1) JEDEC Standard JESD22-A114E, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM), January 2007

2) JEDEC Standard JESD22-C101D, Field-Induced Charged-Device Model (CDM) Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components, October 2008

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Foreign Line Voltages

External voltages applied to the line outputs may cause large currents in the SLIC. The resulting on-chip power dissipation must be limited to prevent thermal destruction if the over-temperature protection cannot react fast enough due to high local power density. The safe power dissipation values are highly dependent on duration. They can be expressed in terms of voltage and current limits directly on the TIP and RING pins (see **Table 18** and **Table 19**).

Table 18 Voltage Limits on Output Pins

Voltage Duration	Pins	Min. Voltage [V]	Max. Voltage [V]
Continuous	TIP, RING	V_N - 0.4	+5
< 10 ms	TIP, RING	V_N - 5	+10
< 100 µs	TIP, RING	V_N - 10	+20
< 1 µs	TIP, RING	V_N - 15	+40

Table 19 Current Limits on Output Pins

Current Duration	Pins	Min. current [A]	Max. current [A]
Continuous	TIP, RING	-0.1	0.1
< 10 ms	TIP, RING	-0.5	0.5
< 100 µs	TIP, RING	-1.0	1.0
< 1 µs	TIP, RING	-1.5	1.5

The above limits should be regarded as typical. They are valid simultaneously and, together with external circuitry, determine the protection requirements.

7.3 Operating Range

V_{GND} = V_{BGND} = 0 V

Table 20 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltages at VDD15, VDD1V5, VDD15P referred to GND	–	1.425	1.5	1.575	V	–
Supply voltages at VDD33, VDD3V3 referred to GND	–	3.135	3.3	3.465	V	–
Supply voltages at VDDP33 referred to GND	–	1.71	–	3.465	V	–
Supply voltages at VDDSWD referred to GND	–	3.135	–	5	V	–
Analog test, filter and gain pins	–	0	–	3.3	V	V_{DD3V3} = 3.3 V, V_{DD1V5} = 1.5 V
Analog pin for passive devices CREF referred to the corresp. ground pin	–	0.5	0.7	0.9	V	V_{DD1V5} = 1.5 V
Ambient temperature under bias	T_A	-40	–	85	°C	–
Junction temperature under bias[1)]	T_J	–	–	125	°C	–
Digital Input/Output Pins (I/O pins, DCDCIO pins)						
High-level input voltage	V_{IH}	2.0	–	3.6	V	$V_{OUT} \geq V_{OH}$ (min)
Low-level input voltage	V_{IL}	-0.3	–	0.8	V	$V_{OUT} \leq V_{OL}$ (max)
High-level output voltage	V_{OH}	2.4	–	–	V	I_{OH} = -3 mA
Low-level output voltage	V_{OL}	–	–	0.4	V	I_{OL} = 3 mA
Average input leakage current per pin	I_{IL}	–	–	20	µA	V_{DD33} = 3.3 V, V_{GND} = 0 V; all other pins are floating, V_{IN} = 0 V or 3.3 V
Input capacitance on digital signal pins	–	–	–	5	pF	–
Input transition rise or fall time on digital signal pins	–	0	–	5	ns	–
Output transition rise or fall time on digital signal pins	–	–	–	7.4	ns	$C_{Load,max}$ = 50 pF
Analog Input Pins (MT, MR)						
Analog input pins referred to ground	–	0.3	–	2.7	V	V_{DD3V3} = 3.3 V
Generated battery voltage	V_N	-150	–	-12	V	–

1) Operation up to 150°C is possible. However, a permanent junction temperature exceeding 125°C could degrade device reliability.

7.3.1 Thermal Resistance

Table 21 Thermal Resistance PG-VQFN-48

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction to case, top	$R_{th,\ JC\text{-}Top}$	–	17	–	K/W	–
Junction to case, bottom	$R_{th,\ JC\text{-}Bottom}$	–	3	–	K/W	–
Junction to ambient	$R_{th,\ JA}$	–	25	–	K/W	4-layer, 76.2 x 114.3 mm^2 JEDEC board

7.3.2 Power-On Sequence

There are no specific requirements for the power-on sequence for the VDD15, VDD1V5, VDD33, VDD3V3, and VDDP33 voltages. The signal voltages must not be applied until the supply voltages on the above mentioned pins are stable.

7.4 DC Characteristics

Table 22 DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line Termination (TIP, RING)						
DC line voltage drop (see **Figure 9**)	$-V_N - V_{TR,\ max}$	–	2.5	3	V	$I_{Trans,DC}$ = 20 mA T_A = 25°C[1] Mode: **ACTIVE**, **RING_BURST**
Output current limit	$\lvert I_{R,\ max}\rvert$, $\lvert I_{T,\ max}\rvert$	70 80	85 100	100 120	mA mA	V_T, V_R = 0 (sinking) V_T, V_R = V_{Nx} (sourcing) Temp = 25°C[2]
Output resistance SLIC at tip	$R_{Int,Tip}$	17	20	23	Ω	T_A = 25°C[3]
Output resistance SLIC at ring	$R_{Int,Ring}$	17	20	23	Ω	T_A = 25°C[3]

1) The systematic temperature dependence is appr. +7 mV / °C
2) The systematic temperature dependence is appr. -0.3% / °C
3) The systematic temperature dependence is appr. +0.1% / °C.

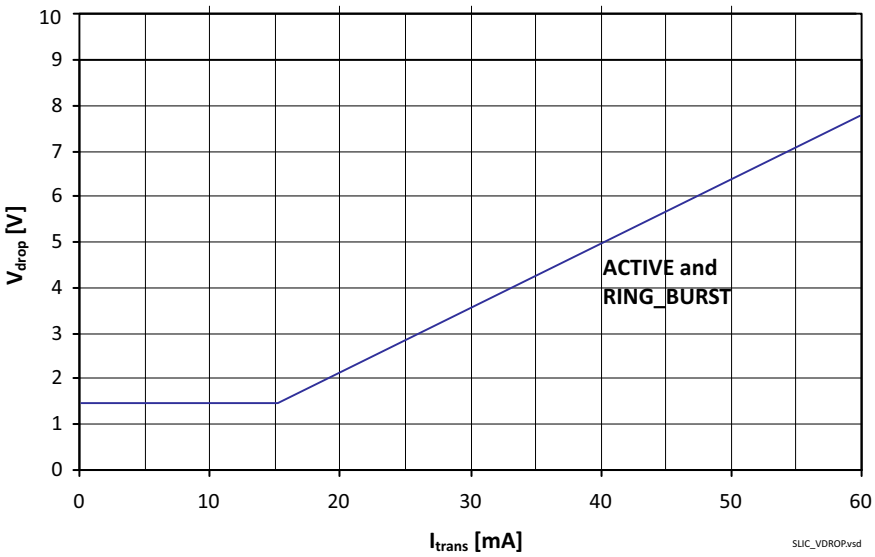


Figure 9 Typical Voltage Drop on Tip and Ring Buffers in Operating Modes ACTIVE and RING_BURST

7.5 AC Characteristics

Table 23 AC Characteristics TIP, RING

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop)	$LTRR_{loop}$	54	60	–	dB	300 Hz < f < 1 kHz
		52	60	–	dB	f = 3.4 kHz
Transversal to longitudinal rejection ratio V_{TR}/V_{long}	$TLRR$	–	50	–	dB	300 Hz < f < 3.4 kHz
Power supply rejection ratio	$PSRR$					$V_{SupplyAC}$ = 100 mVp,
VS/V_{TR}		50	60	–	dB	300 Hz < f < 3.4 kHz
VN/V_{TR}		40	60	–	dB	

*Note: If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA in **ACTIVE** mode; load resistor R_{Load} is 600 Ω.*

7.6 Supply Current and Power Dissipation

The values in **Table 24** and **Table 25** are valid for T_A = 25 °C. The line voltage V_{TR} is set to 40 V and the overhead voltage V_{OVH} is set to 5 V.

Table 24 VN Currents for SLC210 (TIP-RING Open)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VN current **STANDBY**	$I_{N,STBY}$	–	0.25	–	mA	Excludes the current through R_M
VN current **ACTIVE**	$I_{N,ACT}$	–	3.2	–	mA	Open loop, includes the current through R_M
		–	2.3	–	mA	With Automatic Sense Bias Enabled (XTCOS)
VN current **RING_BURST**	$I_{N,RINGING}$	–	3.2	–	mA	Open loop, includes the current through R_M

Table 25 VDD33 and VDD15 Currents for SLC210 (TIP-RING Open)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VDD33 current **DISABLED**	$I_{DD33,DIS}$	–	0.5	–	mA	–
VDD33 current **STANDBY**	$I_{DD33,STBY}$	–	1.0	–	mA	Internal fixed voltage used: 28 V or 45 V
			3.6			Programmable standby voltage from DC/DC DAC
VDD33 current **ACTIVE**	$I_{DD33,ACT}$	–	18	–	mA	–
VDD33 current **RING_BURST**	$I_{DD33,RINGING}$	–	18	–	mA	–
VDD15 current **DISABLED**	$I_{DD15,DIS}$	–	7	–	mA	–
VDD15 current **STANDBY**	$I_{DD15,STBY}$	–	7	–	mA	–
VDD15 current **ACTIVE**	$I_{DD15,ACT}$	–	29	–	mA	–
VDD15 current **RING_BURST**	$I_{DD15,RINGING}$	–	25	–	mA	–

Power dissipation is always a key parameter in modern dense board designs, but it is particularly important in a highly integrated approach such as the SLC210. Whereas the VDD supply currents given above cause a constant on-chip dissipation P_{QDD}, the situation is slightly more complex with the generated battery supply voltage V_N. Power P_{VN} consists of the quiescent power P_{QN} due to V_N bias currents (see **Table 24**) and additional power resulting from any DC line current $I_{L,DC}$. This component P_L consists of a part P_O dissipated in the output stage and the load power P_{Load} (load R_L including loop resistance and protection resistors).

$$P_{VN} = P_{QN} + P_L = P_{QN} + P_O + P_{Load} \quad (1)$$

The total power dissipation of the SLC210 is:

$$P_{DIS} = P_{QDD} + P_{QN} + P_O = P_Q + P_O \quad (2)$$

The total power consumption of the SLC210 is:

$$P_{CON} = P_{QDD} + P_{QN} + P_O + P_{Load} \quad (3)$$

Table 26 to Table 29 show examples of quiescent power dissipation values.

Table 26 Power Calculation in STANDBY Mode

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply	40	0.25	10	VN bias current
VN Supply	40	0.04	2	External DC/DC resistor 1 MΩ
VDD 3.3 V Supply	3.3	3.6	12	Low voltage part
VDD 1.5 V Supply	1.5	7.0	11	Low voltage part
VN Supply	40	0.03	1	External measurement resistor 1.5 MΩ
			35	**Total power consumption (P_{CON})**
			32	**SLIC power dissipation (P_{DIS})**

Table 27 Power Calculation in ACTIVE Open Mode

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply	45	2.30	104	VN bias current
VN Supply	45	0.20	2	External DC/DC resistor 1 MΩ ($R3$)
VDD 3.3 V Supply	3.3	18.00	59	Low voltage part
VDD 1.5 V Supply	1.5	29.00	44	Low voltage part
			208	**Total power consumption (P_{CON})**
			206	**SLIC power dissipation (P_{DIS})**

Table 28 Power Calculation in ACTIVE Mode With R_{LINE} = 300 Ω Line Termination

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply	14.5[1)]	3.20	46	VN bias current
VN Supply	14.5	23.00	333	Line current
VDD 3.3 V Supply	3.3	18.00	59	Low voltage part
VDD 1.5 V Supply	1.5	29.00	44	Low voltage part
			482	**Total power consumption (P_{CON})**
	8.6	23.00	197	Power external resistor (R_{LINE} + $2*R_{PROT}$)
			285	**SLIC power dissipation (P_{DIS})**

1) Please refer to Equation (4) shown below.

$$V_N = I_{L,DC} (R_{Int,Tip} + R_{Int,Ring} + 2*R_{PROT} + R_{LINE}) + V_{OVH} = 14.5\ V \quad (4)$$

The following conditions apply to Table 29:
V_{Ring} = 50 V_{RMS}, f_{Ring} = 20 Hz, V_{DC} = 12 V, V_{OVH} = 5 V, Load = 3 US REN.

Table 29 Power Calculation in RING_BURST Mode With 3 REN

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply			1255	VN power
VDD 3.3 V Supply	3.3	18.00	59	Low voltage part
VDD 1.5 V Supply	1.5	25.00	38	Low voltage part
			1352	**Total power consumption (P_{CON})**
			987	Power external load
			365	**SLIC power dissipation (P_{DIS})**

Table 30 summarizes the calculation of ring power components.

Table 30 Calculation of Ring Power Components

Mode	Load	VN [V]	P_{QN} [mW]	P_O [mW]	P_{Load} [mW]
RING_BURST[1)]	Ringer equiv. $Z = R_L + 1/j\omega C = Z_L e^{i\varphi}$	Tracking supply[2)]: $V_N(t) = -\lvert V_{Ring}(t) + V_{DC}\rvert - V_{OVH}$	$-2/\pi * V_{N,peak} * I_{N,ACT}$	$2/\pi * V_{Ring,peak} / Z_L * V_{OVH}$	$(V_{Ring,peak})^2 * \cos\varphi / (2*Z_L)$

1) Sinusoidal ringing with peak ring voltage $V_{Ring,peak}$ and DC voltage V_{DC}; power values are time averages.

2) For further details refer to the description of quasi-balanced ringing in the System Description [1].

The power required from the VS supply, P_{VS}, can also be calculated. VS has to deliver the total VN power P_{VN} plus all the losses arising from the DC/DC conversion, P_{Loss}. These include the losses in the external converter parts (switch transistor, inductor, capacitor and diode). Thus:

$$P_{VS} = P_{VN} + P_{Loss} = P_{VN} / \eta \quad (5)$$

This can be regarded as a definition of efficiency η. As P_{Loss} includes some virtually constant components (for example SLIC bias current, switching losses), the efficiency depends on power, degrading at low P_{VN} values. Furthermore it depends on the switch transistor, the inductor, the operation mode and the switching frequency. Typical efficiency values range from 60 to 85%.

The instantaneous power dissipation during ringing varies over the ring period. The relationships given in Table 30 apply to the average power, which together with the efficiency determines the power/current requirements on the VS supply (see Table 31). However, when dimensioning the DC/DC converter components, the maximum power values with respect to the switching cycle must be taken into account. For sinusoidal ring voltages, these differ from the average values by a factor of 2 and π/2, respectively. Table 31 contains both average and peak ring power values.

$$V_{N,peak} = V_{Ring} * \sqrt{2} + V_{DC} + V_{OVH} \quad (6)$$

$$I_{N,peak} = (V_{Ring} / Z) * \sqrt{2} + I_{N,ACT} \quad (7)$$

The total power consumption can be calculated using the following equation:

$$P_{TOT} = P_{VS} + P_{VDD,1V5} + P_{VDD,3V3} \quad (8)$$

Table 31 Calculated Typical P_{VS} and Total Power Consumption

Mode	Load /Conditions	P_{VN} [mW]	Efficiency	P_{VS} [mW]	IS_{avg} [mA]	$P_{VDD,1V5}$ [mW]	$P_{VDD,3V3}$ [mW]	P_{TOT} [mW]
STANDBY	**Table 26**	13	0.5	25	2	11	12	48
ACTIVE, open	**Table 27**	106	0.65	162	14	44	59	265
ACTIVE, 300 Ω	**Table 28**	379	0.7	542	45	44	59	645
RING_BURST, average power measured over a ring period	**Table 29**	1255	0.7	1793	149	38	59	1890
RING_BURST, peak power measured in a ring period	**Table 29**	2868	0.7	4097	341	38	59	4194

Table 32 shows measured typical power consumption values in different operating modes for SLC210 with dedicated DC/DC converter. The values assume a loop current I_{TRANS} = 23 mA, R_{LINE} = 300 Ω, 2*R_{PROT} = 72 Ω, V_{LIM} = 40 V.

Table 32 Power Consumption Target Values in Different Op. Modes

Mode	Total Power Consumption (incl. Low voltage part and DC/DC losses)
	SLC210 (dedicated DC/DC)
Low power standby mode measured with fixed on-hook voltage of 28 V (incl. hook detection)	30 mW
Active on-hook (active line feed mode without load)	250 mW
Active off-hook (feeding 23 mA, 300 Ω)	610 mW
Ringing 60 V_{RMS} open loop, 5 REN with ring current regulation	2237 mW

7.7 DC/DC Converter Characteristics

Table 33 DC/DC Converter Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching frequency **ACTIVE**	$f_{SW,ACT}$	60	–	1024	kHz	The actual frequency depends on the load and the DC/DC converter topology used.
Switching frequency **STANDBY**	$f_{SW,STBY}$	20	–	512	kHz	–
Switch driver output slew rate	SR	–	50	–	V/µs	C_{Load} = 1 nF

Table 34 DC/DC Converter Output Voltage V_N

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_N range	–	-150	–	-12	V	Mode: **RING_BURST**
Signal headroom	V_{OVH}	5	–	12	V	Mode: **ACTIVE**, **RING_BURST**
DC/DC converter output voltage	V_N	-24	-22	-20	V	V_{LIM} = 17 V; V_{OVH} = 5 V V_N= V_{LIM}[1)] + V_{OVH} = 17 + 5 = 22 V Mode: **ACTIVE**
		-47.5	-45	-42.5	V	V_{LIM} = 40 V; V_{OVH} = 5 V V_N= V_{LIM} + V_{OVH} = 40 + 5 = 45 V Mode: **ACTIVE**
		–	28	–	V	Use fixed voltage instead of DC/DC DAC, V_{STBY} set to 28 V Mode: **STANDBY**
		–	45	–	V	Use fixed voltage instead of DC/DC DAC, V_{STBY} set to 45 V Mode: **STANDBY**

1) In **ACTIVE** off-hook mode, V_{LIM} is the regulated SLIC output voltage. Please refer to **Equation (9)** shown below.

$$V_{LIM} = I_{L,DC} (R_{Int,Tip} + R_{Int,Ring} + 2*R_{PROT} + R_{LINE}) \quad (9)$$

8 Hardware Design Guidelines

The guidelines below serve as a reference for the design of applications using the SLC210. They are intended to help the reader become familiar with the SLC210 devices and to accelerate the development process. These design and layout guidelines aim at achieving optimum performance for a POTS application. Following these guidelines helps to ensure a reliable design.

8.1 Power Supply and Grounding

8.1.1 Low Voltage Part Supply

The low voltage part of the SLC210 chip requires two supply voltages: +3.3 V and +1.5 V[1]. The tolerance of these supply voltages is ±5%.

The following supply voltages are used to supply digital sections of the SLC210:

- VDDP33: Digital supply for I/O pads (+3.3 V)
  2.5 V or 1.8 V can optionally be used for the I/O pads
- VDD33: Digital supply for DC/DC converter (+3.3 V)
- VDD15: Power supply for digital parts (+1.5 V)

The following supply voltages are used to supply analog sections of the SLC210:

- VDD3V3: Analog supply for channel A and B (+3.3 V)
- VDD1V5: Analog supply voltage for both channels (+1.5 V)
- VDD15P: PLL supply voltage (+1.5 V)

The analog supply voltages must be kept separate from the digital supply and only connected at a central point in the design. In addition, and only if Enhanced Idle Channel Noise requirements need to be met, the digital and analog supplies should be connected via LC filters or ferrite beads (140 Ω @ 100 MHz, 0.55 Ω DC, 200 mA). The analog supply voltages do not have to be generated locally.

The power supply pins of the PLL are described in **Chapter 8.1.3.3**.

For a calculation of the maximum power consumption of the SLC210, see **Chapter 7.6**.

8.1.2 SLIC Part Supply

The SLIC requires a V_N voltage that depends on the line feeding conditions and operating modes. This supply voltage is within the range -12 V down to -150 V, and is generated by a DC/DC converter where the PWM controller is located at the SLC210. The DC/DC converter itself requires an unregulated power supply that depends on the DC/DC converter topology. Typical VS voltages are +12 V and -48 V. In the case of a 12 V supply, the power supply needs to be blocked with at least 22 µF. Please refer to the reference schematics and the DC/DC Converter Externals Application Note **[4]** for details on other DC/DC converter topologies.

The highest power consumption occurs during ring trip. In the case of DC ring trip, it may take up to two ring periods for off-hook to be detected, resulting in an extended period of high power consumption. The fast ring trip feature of the SLC210 should be used to reduce this high power consumption period, and therefore to reduce the cost of the power supply.

1) 1.5 V is either supplied from an external source or from the integrated 1.5 V regulator (see **Chapter 1.2**).

8.1.3 Supply Filtering

8.1.3.1 Supply Concept

The parasitic capacitances to digital ground (GND) must be minimized for analog pins. The principle of this power supply concept is shown in **Figure 10**.

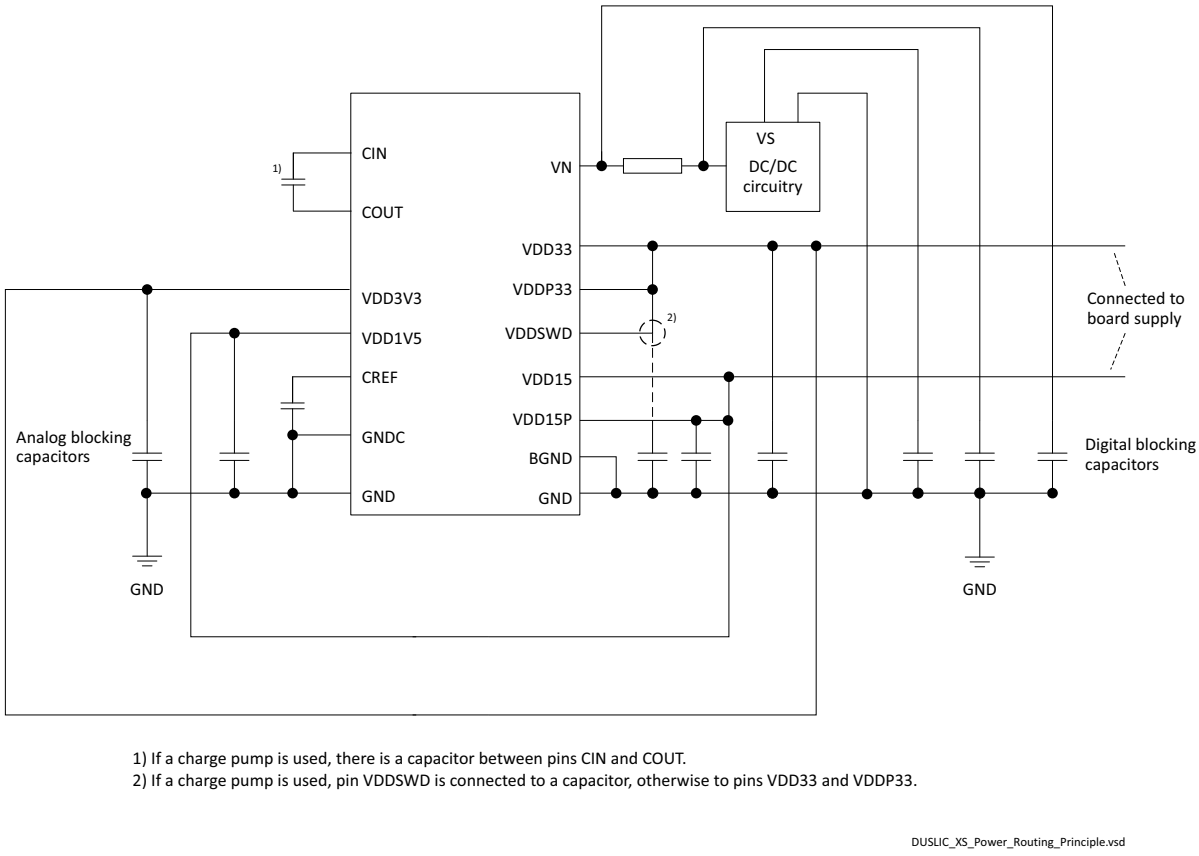


Figure 10 Supply Concept

8.1.3.2 Decoupling the Supply Voltages

The following capacitors are recommended for the SLC210 device:

Table 35 Required Decoupling Capacitors

Supply Pin Group	Decoupling Capacitor
Core supply pins (VDD15)	100 nF ceramic capacitors on each supply pin
Digital interface supply pins (VDDP33)	
Digital supply voltage (VDD33)	2.2 µF and 100 nF in parallel on the supply pin referred to GND
Analog +1.5 V supply pins (VDD1V5)	2.2 µF on each supply pin referred to ground
Analog +3.3 V supply pins (VDD3V3)	2.2 µF and 100 nF (ceramic) in parallel on each supply pin referred to ground
PLL supply pin (VDD15P)	100 nF directly at the pin
DC/DC converter supply (VS)	one capacitor of at least 22 µF (placed near the power pins)
SLIC supply (VN)	2.2 µF, low ESR
Charge pump (optional)	2*100 nF ceramic capacitor (between pin VDDSWD and GND, and between pins CIN and COUT)

8.1.3.3 PLL Supply Voltage (VDD15P)

VDD15P supplies an analog section of the low voltage part, but is filtered against the digital ground to avoid disturbance of the other analog supplies. A blocking capacitor of 100 nF against digital ground (GND) must be placed directly on the pin VDD15P to filter high frequency power supply noise. VDD15P is directly connected to the +1.5 V digital power supply rail.

8.1.3.4 Charge Pump Function (VDDSWD)

The charge pump function allows the support of standard level MOS transistors with no external driver stage. The internal charge pump is connected to three pins CIN, COUT and VDDSWD. When no charge pump is used, VDDSWD must be connected to VDD33 and CIN, COUT must be left unconnected.

When the charge pump is used, a 100 nF capacitor is connected between VDDSWD and GND, and a second 100 nF capacitor must be connected between CIN and COUT.

8.2 Layout Recommendations

In all the figures in this chapter, the analog channel specific decoupling capacitors are shown, whereas the decoupling capacitors for the digital power supplies are not shown.

8.2.1 Placement

8.2.1.1 Placement Hints for the Digital Part

- Place decoupling capacitors as close as possible to the supply pins of the SLC210 and each associated ground pin.
- The decoupling capacitor of the PLL must be placed as close as possible to the device.
- In order to reduce reflections the following mounting options for the SLIC interface and clock signal should be considered (especially for long or branching lines). For the CLKI and RX, TX signals, an AC termination to ground (for example 470 Ω in series with 10 pF) is recommended on the SLC210 (receive side) to avoid distortion. A serial termination (33 Ω) is needed on the transmitter side.
- Pull-up resistors for the interrupt signals (INT) must only be placed once in the system.

8.2.1.2 Placement Hints for Analog Part

This chapter refers to the typical external components shown in **Figure 7** and the recommended DC/DC converter application circuit shown in **Figure 8**.

- C_{REF} should be placed as close as possible to the CREF pin since this filters the on-chip reference voltage.
- The voltage sense resistor for the DC/DC converter should be placed as close as possible to the VSENSE input pin. A maximum wire length of 5 mm is allowed, and the wire should not be close to the ground plane.
- The blocking capacitors should be placed as close as possible to the respective pins of the device.
- C_{DC} must be placed close to the SLC210.
- The resistors R_{PROT} and capacitors C_{STAB} (see **Figure 7**) can be placed near to the SLIC or near to the protection components. The wires (tip and ring) must be routed in parallel, as differential lines, between the protection components and the SLIC.
- The centralized capacitor for the SLIC supply $C2$ must be placed at the power connector, VS (see **Figure 11**).
- The blocking capacitor should be at least 22 µF and must be placed close to the input pins of the DC/DC converter circuitry (see **Figure 11**).
- The components of the DC/DC converter circuit must be placed close together. The area has to be as small as possible to avoid disturbances.
- The switching transistor needs a heat sink of at least 100 mm^2.
- The value for the sense resistor $R2$ in the recommended default schematic (see **Figure 8**) depends on the DC/DC converter type used. A value of 0.082 Ω should be used for the standard application with dedicated DC/DC converter control for each SLIC channel. When using combined DC/DC converter control, a value of 0.068 Ω should be used for the sense resistor.
- The traces of the circuitry between pin VNx and the inductor $L1$ (including the two 220 nF capacitors) must have a width of min. 1.5 mm.
- The 2.2 µF capacitor at the VNx supply can be of type X7R or electrolytic. The voltage rating must be chosen according to the application needs. If an electrolytic capacitor is used, it should be of low ESR type to minimize voltage ripple on VN.
- The parts and traces of the DC/DC converter should not be placed near the tip and ring lines, or should be routed in a separate layer.

8.2.2 Routing

General recommendations for the routing:

- The ground of the DC/DC converter circuitry is referred to the digital ground (GND). This signal can be routed as a trace. No plane is required.
- The digital tracks should not cross or be placed parallel to the analog tracks of the SLC210. This especially includes the PCM interface signals and clock signals. Host controller interfaces including the control signals must not to be routed through the analog section. It is recommended that these tracks are routed out of the package on the digital side in an inner layer or on the bottom layer to avoid crosstalk to sensitive analog circuitry.
- The digital host interface and clock signals should be routed on the component and solder side and kept far away from the analog signals.
- The control lines should be routed on the component side (top side).
- The connection to GND, the battery voltages and all the connections to the protection devices must be low impedance in order to prevent ground bouncing due to the high impulse currents in the case of an overvoltage strike - wide tracks or planes are required.

Recommendations for the line side:

- Depending on the protection requirements, the track width from the TIP/RING interface to the external overvoltage protector (if used) must be chosen appropriately. In practice, a trace width of 0.5 mm (20 mil) is sufficient to meet most surge requirements.
- When a layer change is necessary between the line connector and protection device (for example, a TISP element), three vias must be used, as one is not sufficient. This is not necessary between the tip and ring lines and the R_M resistors or to the 15 nF capacitors.
- The connections between the C_{STAB} capacitors and ground must be low impedance.
- Depending on the protection requirements, the resistance R_M may need to be split into more than one component in order to satisfy the maximum voltage rating specification of the components used. In certain cases, two (2 x 750 kΩ) or three (3 x 499 kΩ) resistors in series are recommended.
- Air gap between tip/ring traces from SLC210 shall be at least 0.2 mm (8 mil).
- Air gap of tip/ring traces from SLC210 to any other trace shall be at least 0.2 mm (8 mil).
- Trace with of tip/ring traces from SLC210 to overvoltage protector shall be 0.125 mm (5 mil).
- Trace with of tip/ring traces to R_M resistors shall be 0.1 mm (4 mil).
- Air gap between of tip/ring traces to R_M resistors shall be at least 0.2 mm (8 mil).

Recommendations for the DC/DC converter are:

- The traces for the input voltage of the DC/DC converter must be routed separately for each channel and must be connected near to the power supply at a blocking capacitor (star point).
- The power supplies are placed in the two inner layers on a multi-layer board or in large traces (0.2 mm - 0.3 mm width) on a 2-layer board.
- The components of the DC/DC converters must be placed on the smallest possible area, the traces must have a minimum width and coupling to the analog part must be minimized to avoid noise (**Figure 11**).
  The main current loops for the DC/DC converter during the two switching periods can be described as:
  – Switch on-time: VS blocking capacitor - switch - coil - current sense resistor - VS blocking capacitor
  – Switch off-time: coil - diode - VN filter capacitor - current sense resistor - coil
  The four components $L1$, $R2$, $D1$ and $C3$ must be placed close together on one side of the PCB in order to minimize the current loop.
- Traces for Isense and Vsense* can be as narrow as design rules allow, e.g. 0.1 mm (4 mil).
- Traces for Isense and Vsense* need to be routed in a way to minimize noise pick-up.
- If needed, Isense should be embedded into guard ground traces with smallest possible air gap to both sides, e.g. 0.1 mm (4 mil).

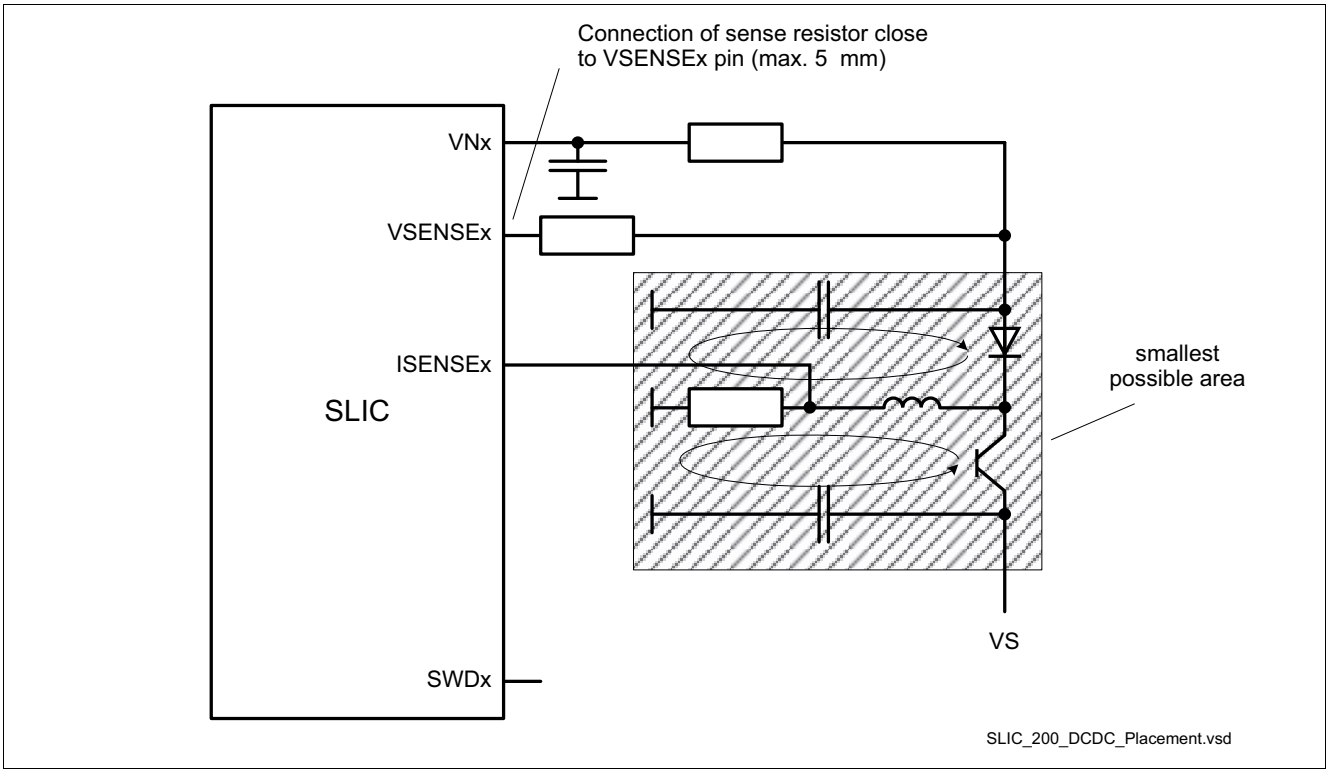


Figure 11 DC/DC Converter Component Placement

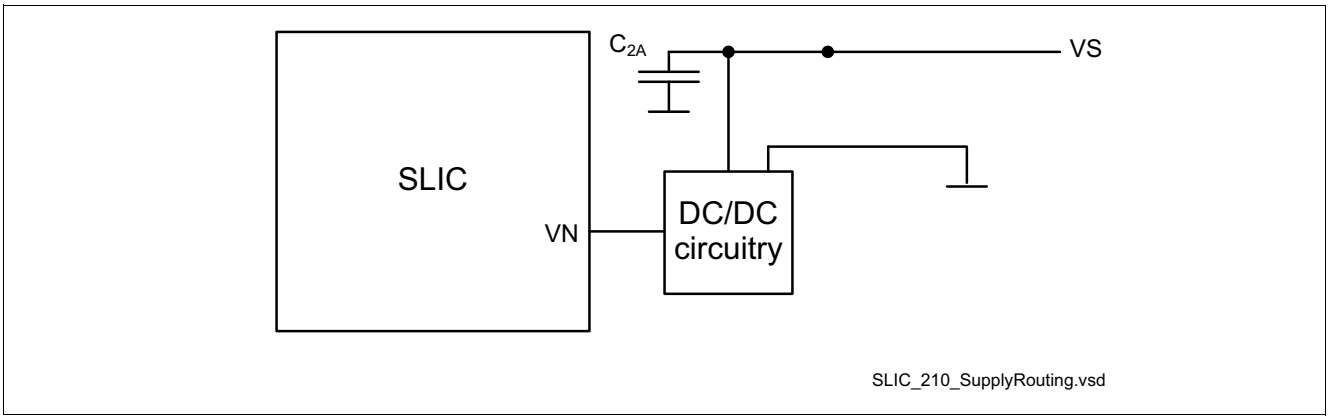


Figure 12 Power Supply Routing for DC/DC Converter Circuitry in the SLC210

9 Package Outline

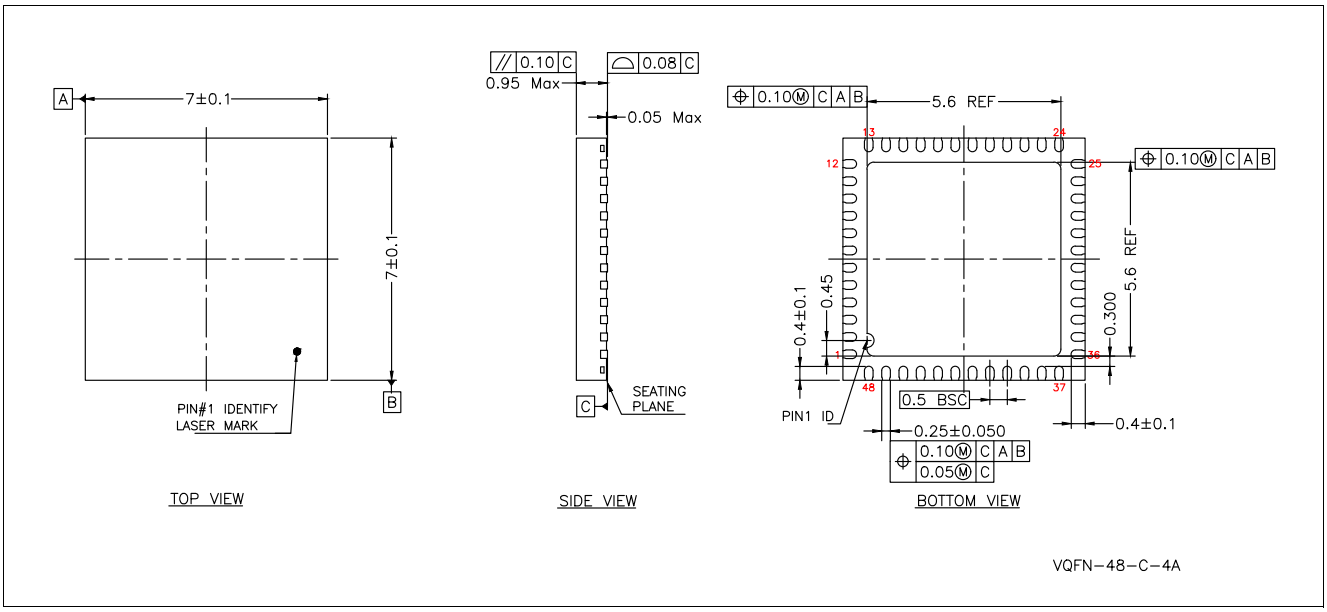


Figure 13 PG-VQFN-48 (Plastic Green Very Thin Profile Quad Flat Non Leaded Package)

Dimensions in mm.

Package description, package handling, PCB and board assembly information is available on request.

Literature References

[1] Gateway SoCs/SLC220/SLC210 FXS Line Interface User's Manual System Description Rev. 2.0, 2017-05-31

[2] Gateway SoCs Voice Processing User's Manual System Description Rev. 3.0, 2016-09-30

[3] SLC220/SLC210 Version 1.1 Protection Requirements Application Note Rev. 2.0, in preparation

[4] SLC220/SLC210 Version 1.1 DC/DC Converter Externals Application Note Rev. 2.0, in preparation

Attention: Please refer to the latest revision of the documents.

Standards References

[5] JEDEC STANDARD JESD51-9, JULY 2000, Test Boards for Area Array Surface Mount Package Thermal Measurements

Terminology

B	
BoM	Bill of Materials
C	
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
CPE	Customer Premises Equipment
E	
ESD	ElectroStatic Discharge
G	
GPIO	General Purpose IO
I	
IO	Input Output
IP	Internet Protocol
J	
JEDEC	Joint Electron Device Engineering Council
N	
NMOS	N-type Metal-Oxide-Semiconductor field effect transistor
P	
PMOS	P-type Metal-Oxide-Semiconductor field effect transistor
POTS	Plain Old Telephone System
PWM	Pulse Width Modulation
R	
REN	Ringer Equivalent Number
S	
SLIC	Subscriber Line Interface Circuit
SME	Small and Medium-sized Enterprises
SSI	Intel® SLIC for linecards Interface